

REASUNOS

RS100N135T

N-Channel Trench Power MOSFET

 Lead Free Package and Finish

General Description

The RS100N135T is SGT MOSFET designed for high current switching applications. Rugged EAS capability and ultra low $R_{DS(ON)}$ is suitable for PWM, load switching applications.

Features

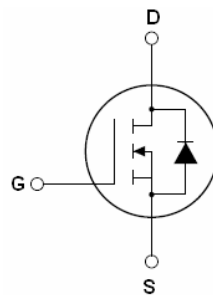
- $V_{DS}=100V$; $I_D=135A$ @ $V_{GS}=10V$;
 $R_{DS(ON)}<5.8m\Omega$ @ $V_{GS}=10V$
- Ultra Low On-Resistance
- High UIS and UIS 100% Test

Application

- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply



To-220 Top View



Schematic Diagram

$$V_{DS} = 100V$$

$$I_D = 135A$$

$$R_{DS(ON)} = 4.8m\Omega \text{ (Typ.)}$$

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
RS100N135T	RS100N135T	TO-220	-	-	-

Table 1. Absolute Maximum Ratings (TA=25°C)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage ($V_{GS}=0V$)	100	V
V_{GS}	Gate-Source Voltage ($V_{DS}=0V$)	± 20	V
I_D (DC)	Drain Current (DC) at $T_c=25^\circ C$	135	A
I_D (DC)	Drain Current (DC) at $T_c=100^\circ C$	105	A
I_{DM} (pulse)	Drain Current-Continuous@ Current-Pulsed (Note 1)	540	A
P_D	Maximum Power Dissipation($T_c=25^\circ C$)	232	W
	Derating Factor	1.55	W/°C
E_{AS}	Single Pulse Avalanche Energy (Note 2)	900	mJ
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 To 175	°C

Notes 1.Repetitive Rating: Pulse width limited by maximum junction temperature

2.EAS condition: $T_J=25^\circ C$, $V_{DD}=40V$, $V_G=10V$, $R_G=25\Omega$

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RS100N135T

Table 2. Thermal Characteristic

Symbol	Parameter	Value	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	---	0.646	$^{\circ}C/W$

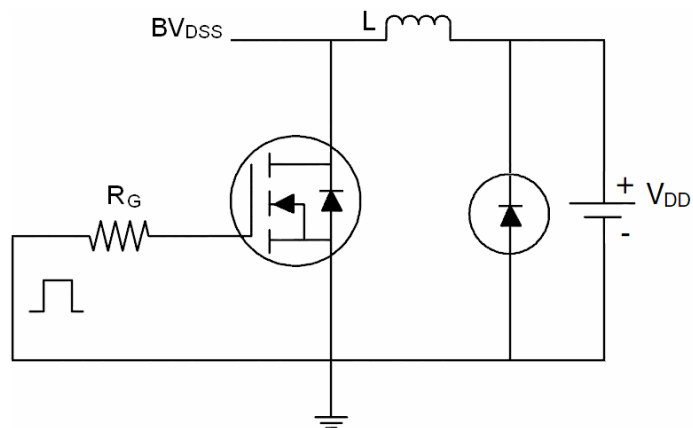
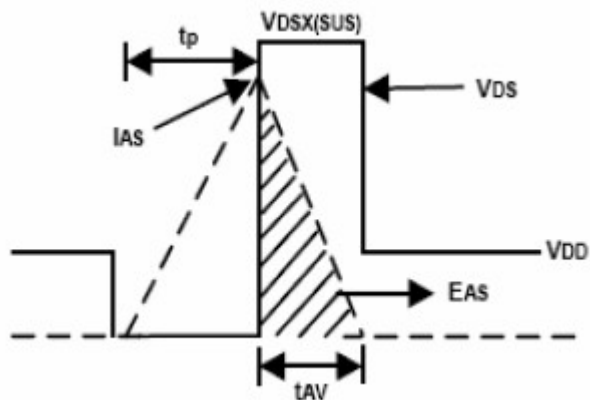
Table 3. Electrical Characteristics (TA=25 $^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On/Off States						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V I _D =250μA	100			V
I _{DSS}	Zero Gate Voltage Drain Current(Tc=25℃)	V _{DS} =100V,V _{GS} =0V			1	μA
I _{DSS}	Zero Gate Voltage Drain Current(Tc=125℃)	V _{DS} =100V,V _{GS} =0V			10	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V,V _{DS} =0V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} ,I _D =250μA	2		4	V
R _{DS(ON)}	Drain-Source On-State Resistance	V _{GS} =10V, I _D =40A		4.8	5.8	mΩ
Dynamic Characteristics						
g _{FS}	Forward Transconductance	V _{DS} =10V,I _D =15A	20			S
C _{iss}	Input Capacitance	V _{DS} =25V,V _{GS} =0V, f=1.0MHz		6750		PF
C _{oss}	Output Capacitance			1020		PF
C _{rss}	Reverse Transfer Capacitance			108		PF
Q _g	Total Gate Charge	V _{DS} =20V,I _D =5A, V _{GS} =10V		98		nC
Q _{gs}	Gate-Source Charge			29		nC
Q _{gd}	Gate-Drain Charge			20		nC
Switching Times						
t _{d(on)}	Turn-on Delay Time	V _{DD} =30V,I _D =40A,R _L =15Ω V _{GS} =10V,R _G =2.5Ω		15		nS
t _r	Turn-on Rise Time			32.3		nS
t _{d(off)}	Turn-Off Delay Time			24		nS
t _f	Turn-Off Fall Time			15		nS
Source-Drain Diode Characteristics						
I _{SD}	Source-drain Current(Body Diode)			135		A
I _{SDM}	Pulsed Source-Drain Current(Body Diode)			540		A
V _{SD}	Forward On Voltage ^(Note 1)	T _J =25℃,I _{SD} =40A,V _{GS} =0V		0.9	0.99	V
t _{rr}	Reverse Recovery Time ^(Note 1)	T _J =25℃,I _F =30A di/dt=100A/μs		45		nS
Q _{rr}	Reverse Recovery Charge ^(Note 1)			80		nC
t _{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible(turn-on is dominated by L _S +L _D)				

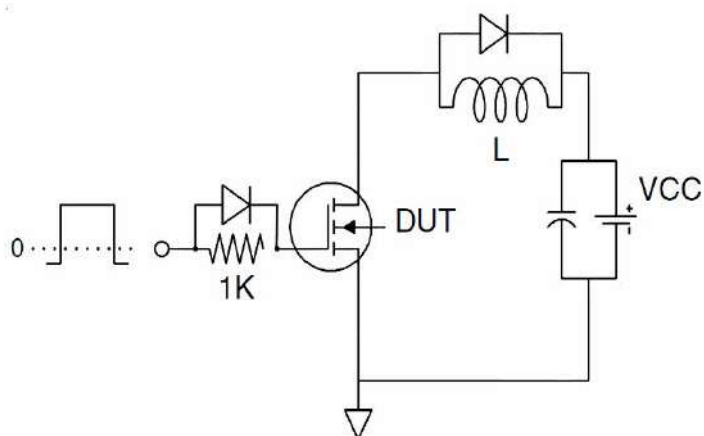
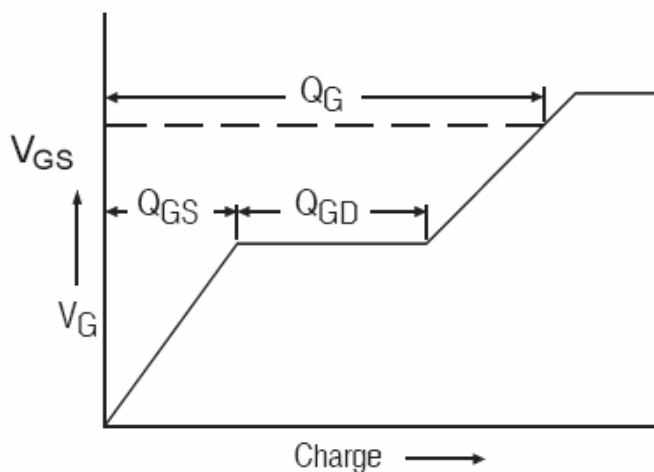
Notes 1. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 1.5\%$, $R_G=25\Omega$, Starting $T_J=25^{\circ}C$

Test Circuit

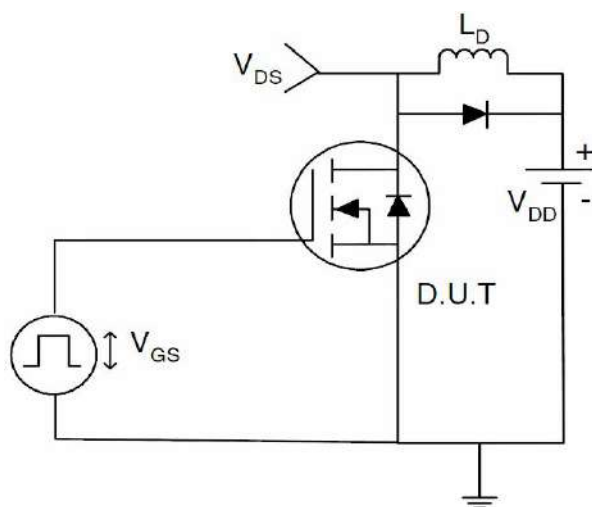
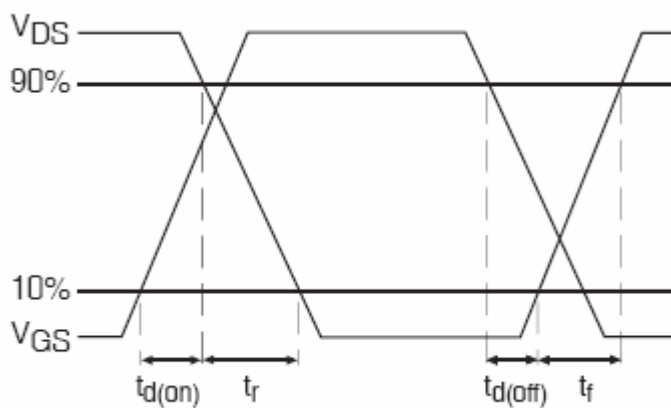
1) E_{AS} Test Circuits



2) Gate Charge Test Circuit:



3) Switch Time Test Circuit:



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (Curves)

Figure1. Output Characteristics

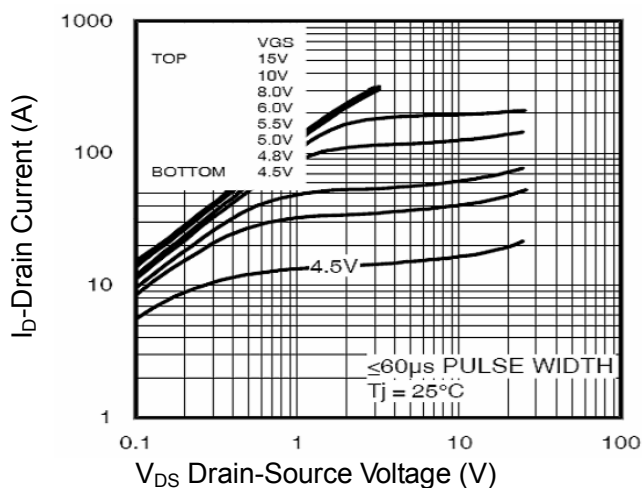


Figure2. Transfer Characteristics

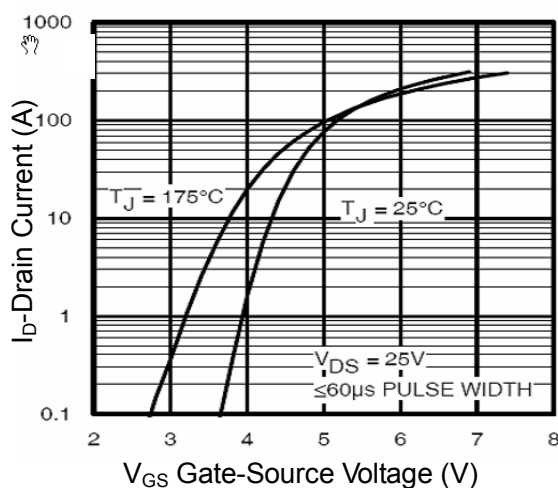


Figure3. BVDSS vs Junction Temperature

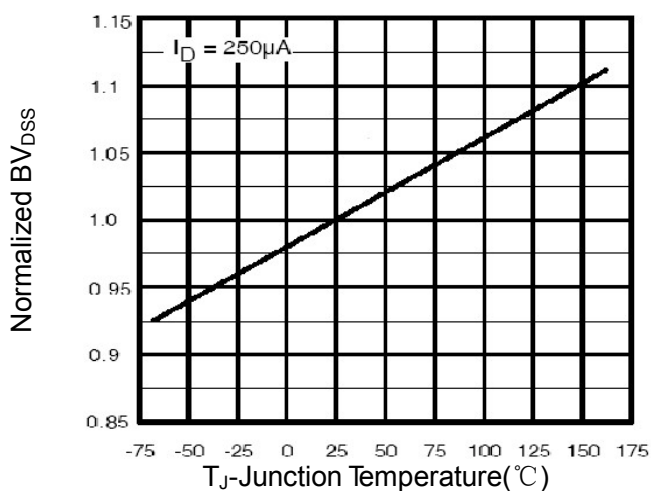


Figure4. ID vs Junction Temperature

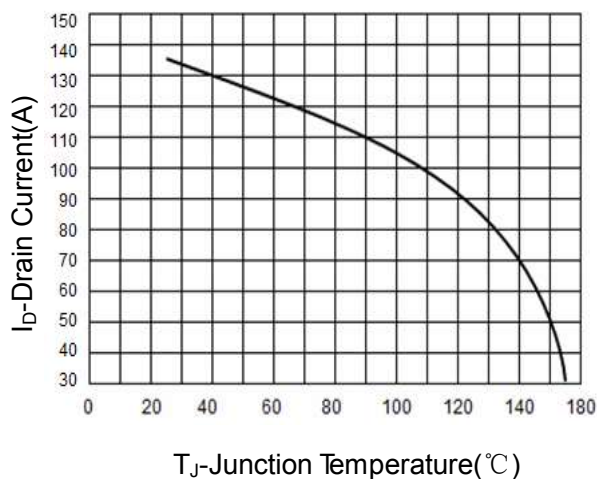


Figure5. VGS(th) vs Junction Temperature

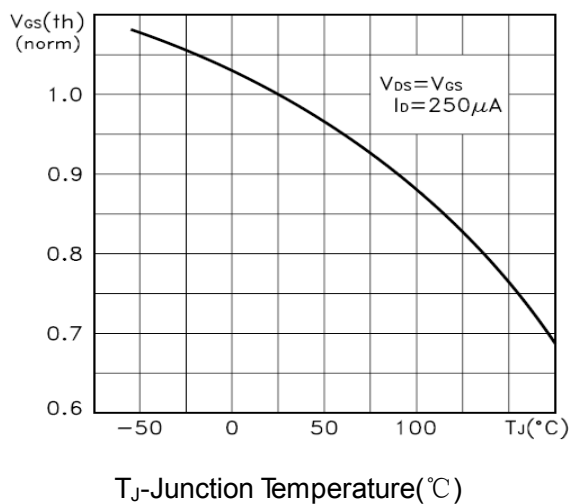
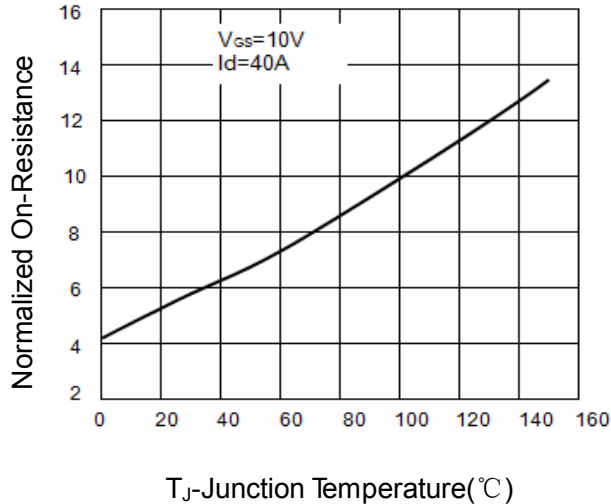


Figure6. Rdson Vs Junction Temperature



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Figure7. Gate Charge

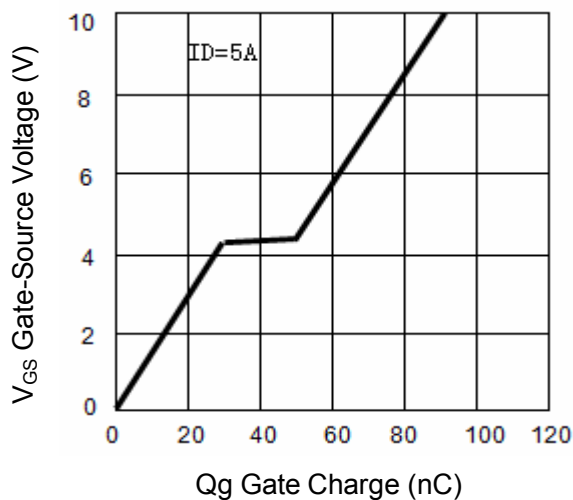


Figure8. Capacitance vs Vds

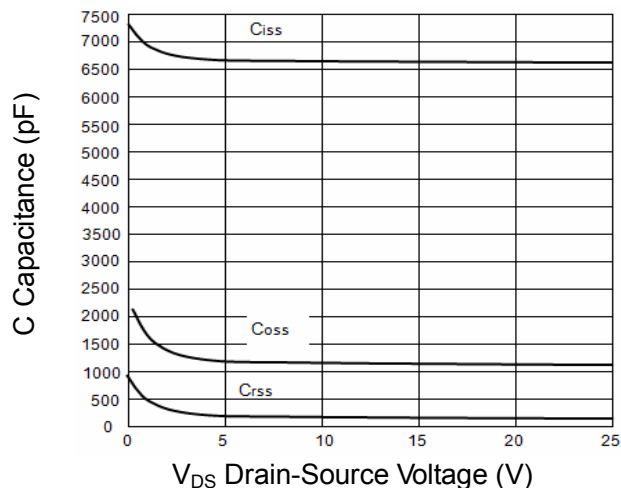


Figure9. Source- Drain Diode Forward

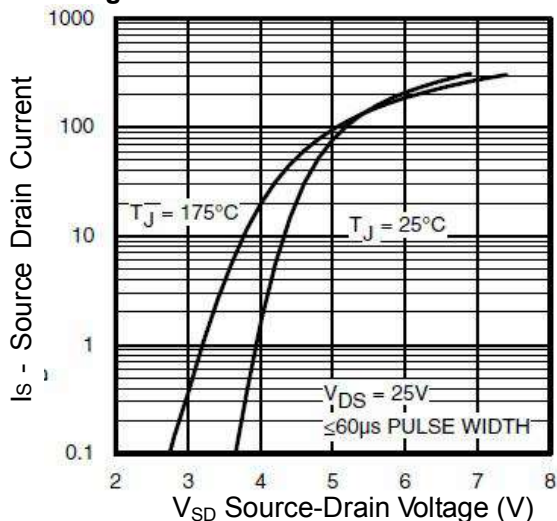


Figure10. Safe Operation Area

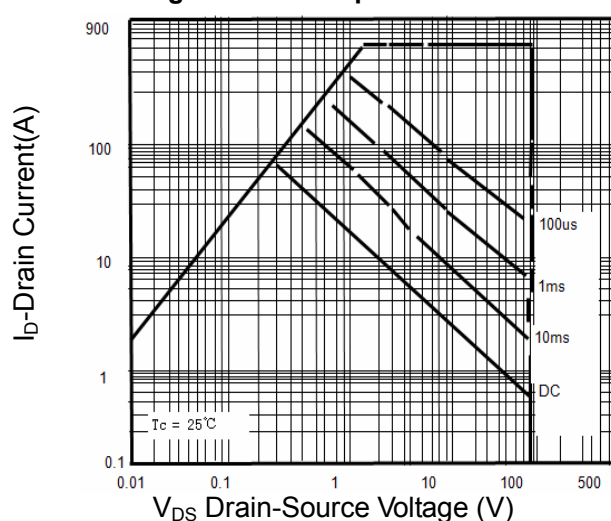
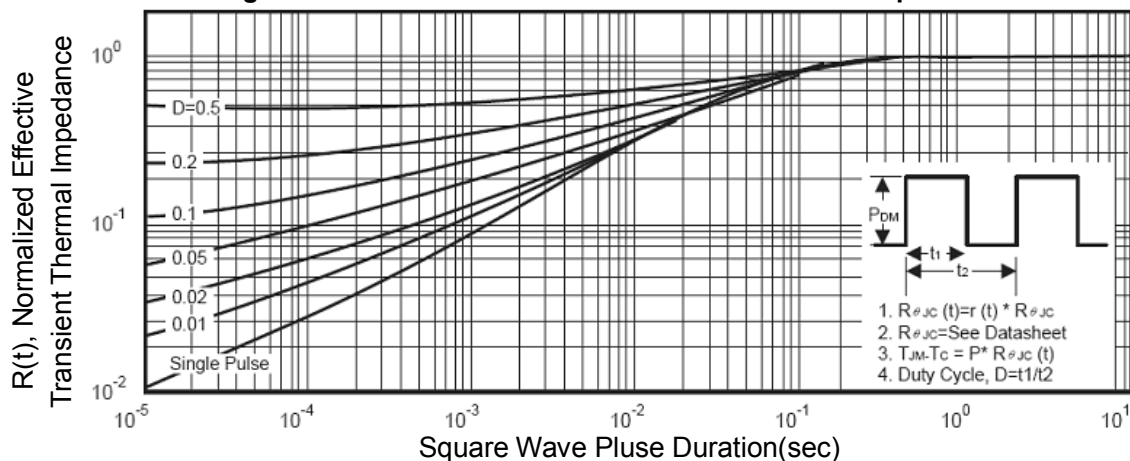


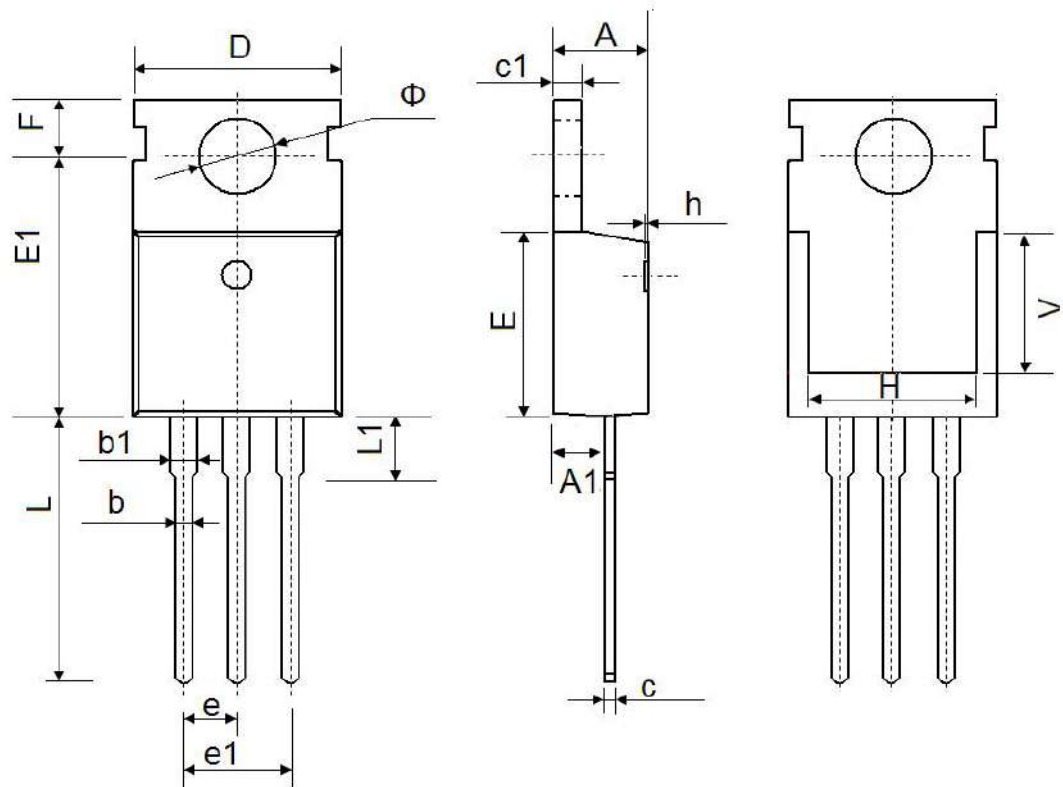
Figure11. Normalized Maximum Transient Thermal Impedance



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TO-220 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max
A	4.300	4.700	0.169	0.185
A1	2.200	2.600	0.087	0.102
b	0.700	0.950	0.028	0.037
b1	1.170	1.410	0.046	0.056
c	0.450	0.650	0.018	0.026
c1	1.200	1.400	0.047	0.055
D	9.600	10.400	0.378	0.409
E	8.8500	9.750	0.348	0.384
E1	12.650	12.950	0.498	0.510
e	2.540 TYP.		0.100TYP.	
e1	4.980	5.180	0.196	0.204
F	2.650	2.950	0.104	0.116
H	7.900	8.100	0.311	0.319
h	0.000	0.300	0.000	0.012
L	12.750	14.300	0.502	0.563
L1	2.850	3.950	0.112	0.156
V	7.500 REF.		0.295 REF.	
Φ	3.400	4.000	0.134	0.157