REASUNOS

RS100N20D

N CHANNEL ENHANCEMENT MODE POWER MOSFET

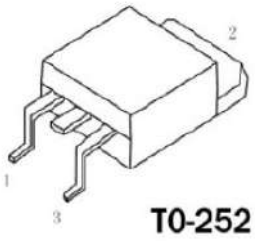
Lead Free Package and Finish

Description:

RS100N20D Series are from Advanced Power MOSFETs innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance,it provides the designer with an extreme efficient device for use in a wide range of power applications.

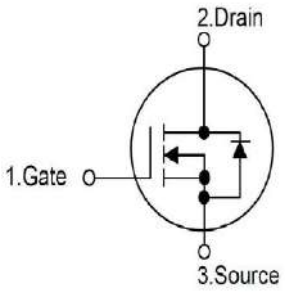
The TO-252 package is widely preferred for all commercial industrial surface mount applications and suited for low voltage application such as DC/DC converters.

I_D	$R_{DS(ON)}$(Max)	V_{DSS}
20A	55mΩ	100V



T0-252

Not to Scale



Features:

- lower Gate Charge
- Simple Drive Requirement
- Fast Switching Characteristic
- RoHS Compliant

Ordering Information

Part Number	Package	Marking
RS100N20D	TO-252	RS100N20D

Absolute Maximun Ratings Tc=25℃ unless otherwise specified

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-Source Voltage	±20	A
I_D @Tc=25℃	Drain Current	20	
I_D @Tc=70℃	Drain Current,Vgs@10V	13.0	
I_{DM}	Pulsed Drain Current (Note*1)	60	
P_D @Tc=25℃	Total Power Dissipation	44.6	W
TL	Maximum Temperature for Soldering Leads at 0.063in(1.6mm)from Case for 10 seconds	300	℃
TPKG	Package Body for 10 seconds	260	
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

Caution:Stresses greater than those listed in the“Absolute Maximum Ratings”Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	Value	Units
Rthj-a	Maximum Thermal Resistance,Junction-ambient*3	62.5	℃/W
Rthj-c	Maximum Thermal Resistance,Junction-case	3.6	℃/W

Electrical Characteristics @TJ=25℃(unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-source Breakdown Voltage	100	--		v	V_{GS}=0V,I_D=1mA
I_{DSS}	Drain-Source Leakage Current	--		25	μA	V_{DS}=80V,V_{GS}=0V
I_{GSS}	Gate-Source Forward Leakage	--	--	100	nA	V_{GS}=20V V_{DS}=0V
	Gate-Source Reverse Leakage	--	--	-100		V_{GS}=-20V V_{DS}=0V
g_{fs}	Forward Transconductance	--	14	--	S	I_D=8A V_{DS}=10V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{DS(on)}$	Static Drain-Source On-Resistance*2	--	45	55	mΩ	V_{GS}=10V,I_D=12A
		--	58	85	mΩ	V_{GS}=5V,I_D=8A
$V_{GS(TH)}$	Gate Threshold Voltage	1	1.5	3	V	V_{GS}=V_{DS},I_D=250μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$t_{d(on)}$	Turn-on Delay Time*2	--	6.5	--	nS	V_{DS}=50V I_D=12A Rg=1Ω Vgs=10V
t_{rise}	Rise Time	--	18	--		
$t_{d(off)}$	Turn-OFF Delay Time	--	20	--		
t_{fall}	Fall Time	--	5.0	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
C_{iss}	Input Capacitance	--	840	1320	pF	V_{GS}=0V V_{DS}=-25V f=1.0MHz
C_{oss}	Output Capacitance	--	115	--		
C_{rss}	Reverse Transfer Capacitance	--	80	--		
Q_g	Total Gate Charge*2	--	13.5	20.5	nC	V_{DS}=80V I_D=12A V_{GS}=4.5V
Q_{gs}	Gate-Source Charge	--	3	--		
Q_{gd}	Gate-Drain("Miller"）Charge	--	1.6	--		

Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V_{SD}	Diode Forward Voltage*[2]	--	--	1.3	V	I_S=12A,V_{GS}=0V
t_{rr}	Reverse Recovery Time*[2]	--	41	--	nS	V_{GS}=0V I_S=12A,di/dt=100A/μs
Q_{rr}	Reverse Recovery Charge	--	70	--	nC	

Notes:

*1.Pulse width limited by max.junction temperature
*2.Pulse test
*3.Surface mounted on 2 in^2 copper pad of FR4 board,

Typical Feature curve

Figure1.Typical Output Characteistics

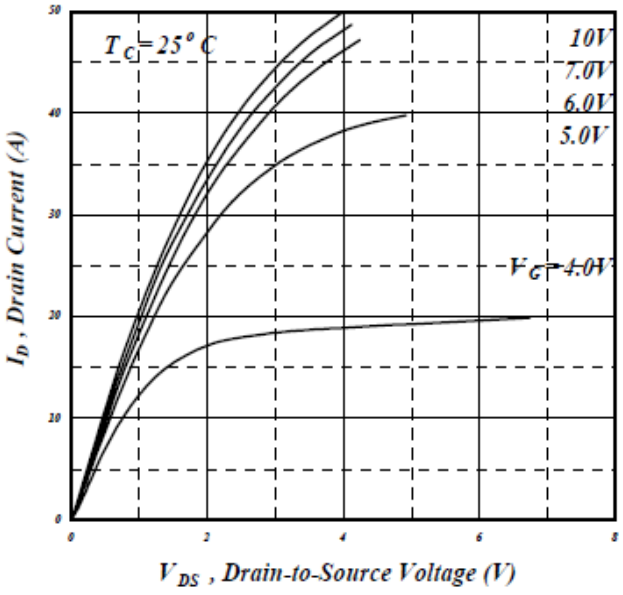
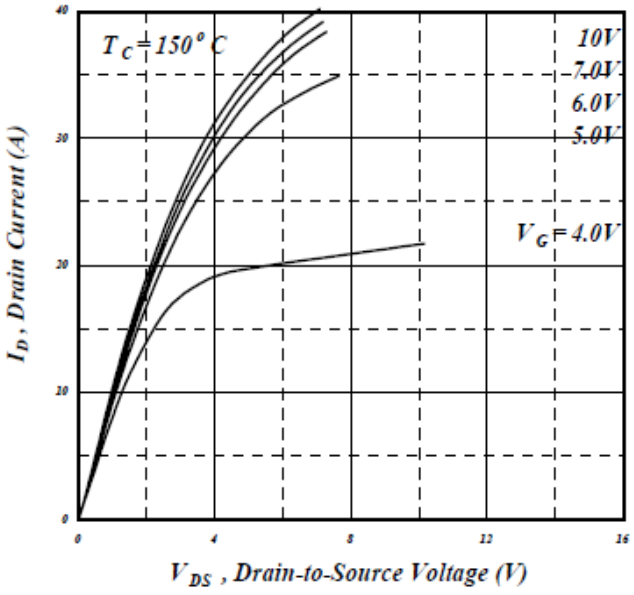
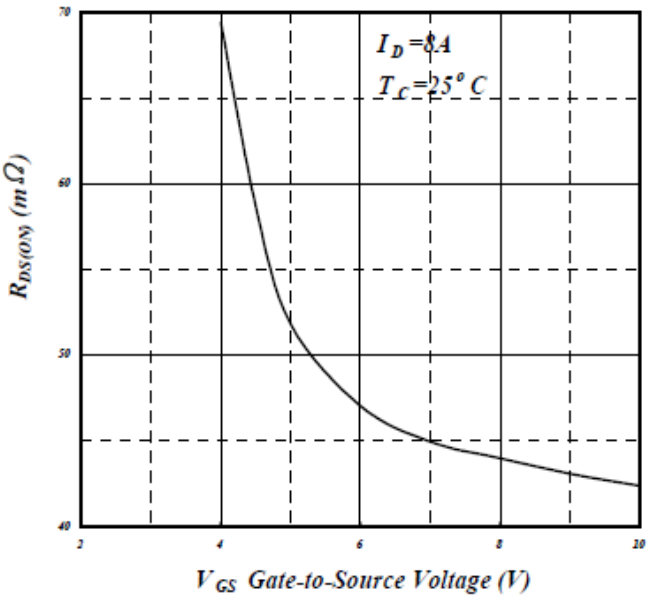


Figure2.Typical Output Characteristics



Figuer3.Typical ON Resistance V.S Gate Voltage



Figuer4.Normalized On-Resistance V.S.Junction Temperature

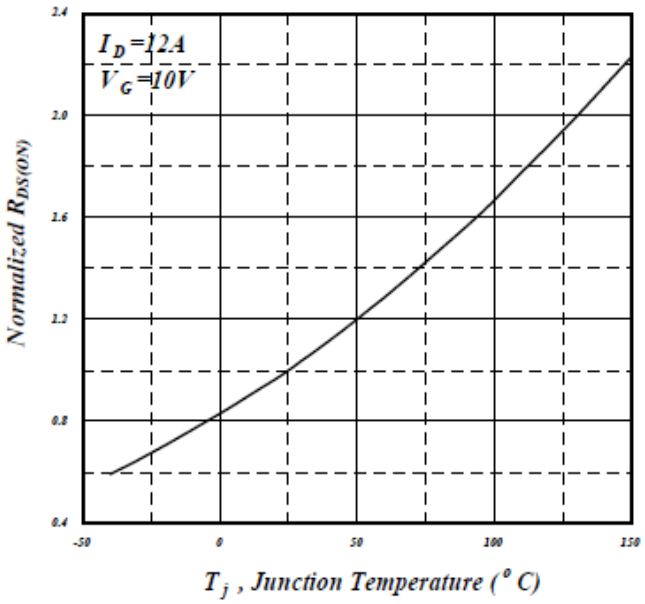


Figure5.Forward Characteristic of Reverse Diode

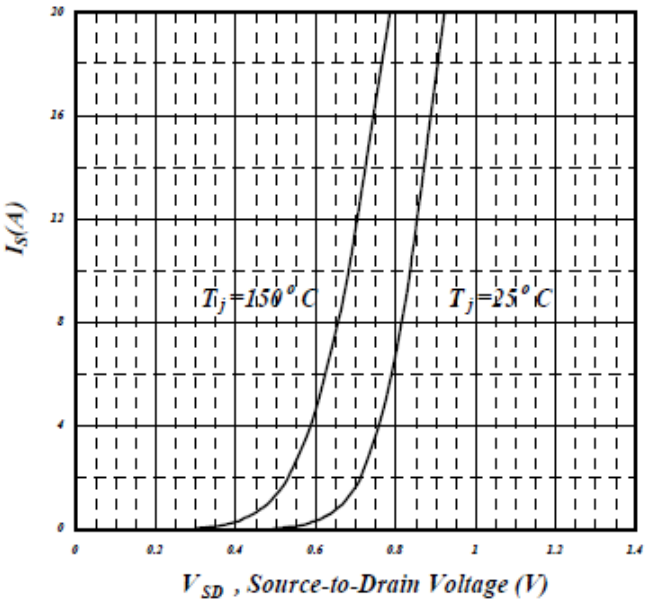


Figure6.Gate Threshold Voltage V.S Junction Temperature

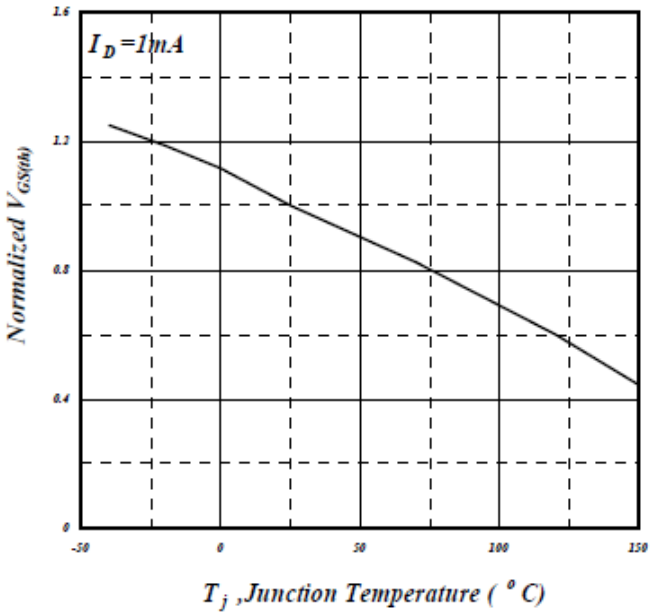


Figure7. Gate Charge Characteristics

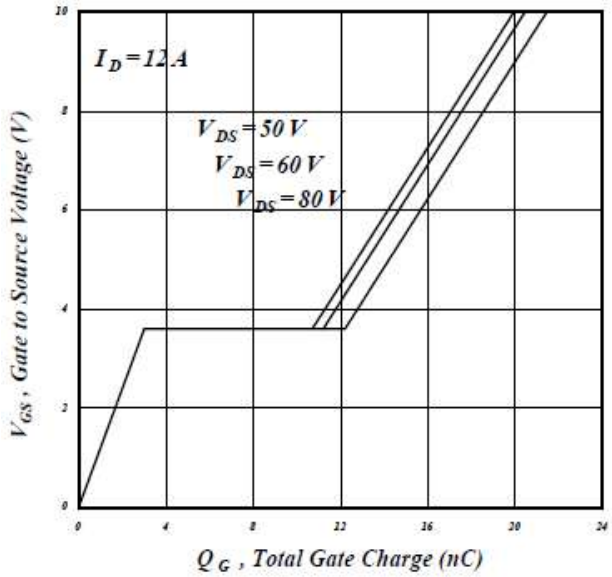


Figure8.Typical Capacitance Characteristics

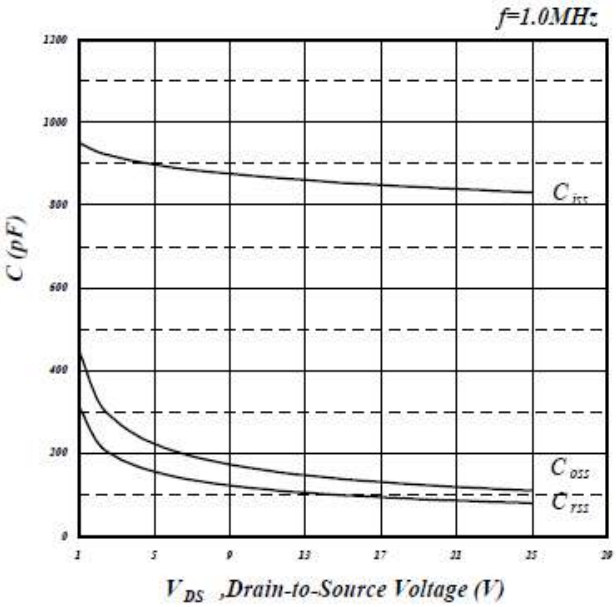


Figure9.Maximum Safe Operating Area

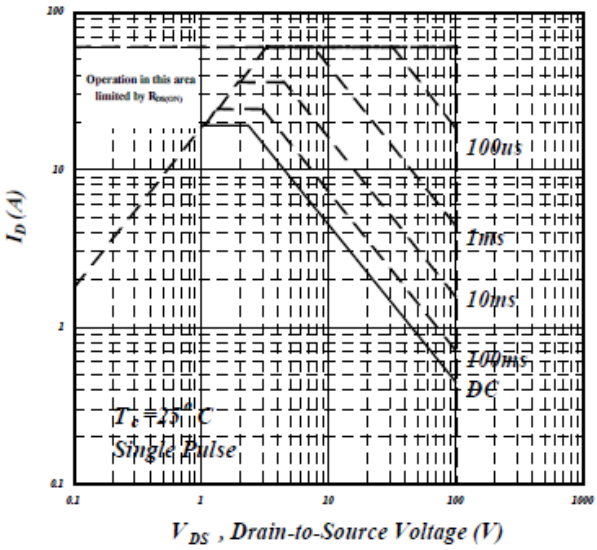


Figure10.Effective Transient Thermal Impedance

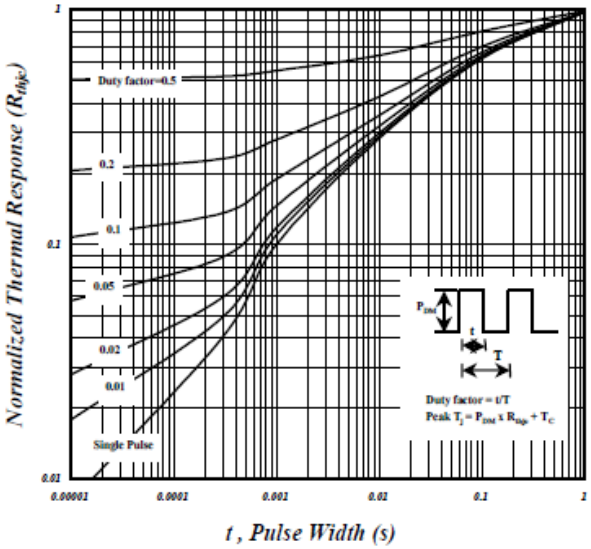


Figure11.
Switching Time Waveform

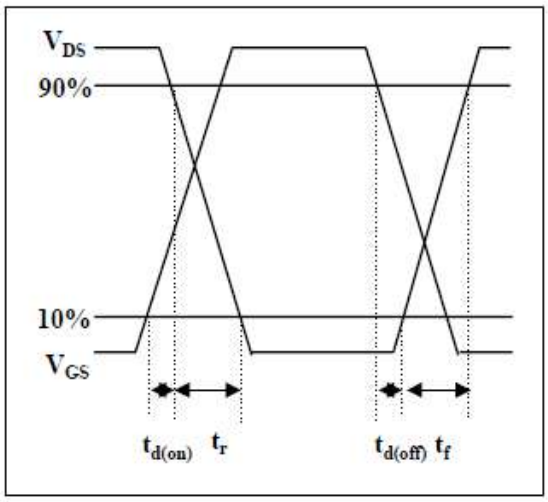
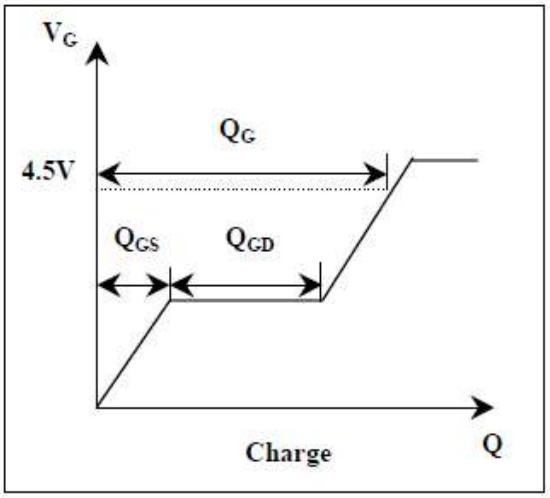
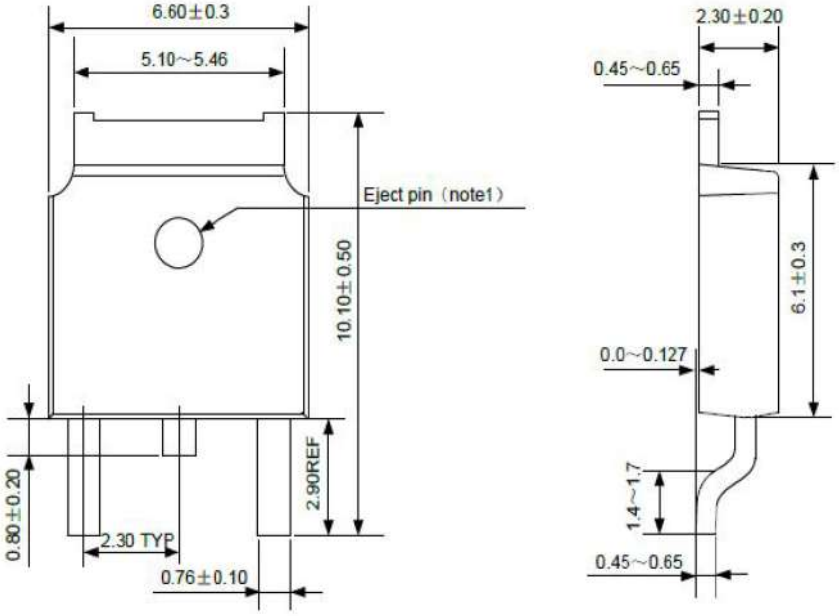


Figure12.
Gate Charge Waveform



Package Outline: TO-252 FOOTPRINT

Unit:mm



Note: The location is divided into top pinhole with no top pinhole two conditions

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