REASUNOS

RS100N85G

N-Channel Enhancement Mode MOSFET

Lead Free Package and Finish

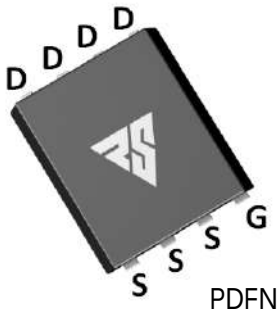
I_D	$R_{DS(ON)}$(TYP.)	V_{DSS}
85A	5.8mΩ	100V

Applications:

- High Frequency Switchin
- Synchronous Rectification

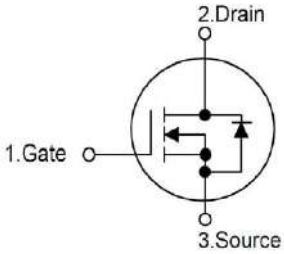
Features:

- V_{DS}=100V; ID=85A@ VGS=10V
- $R_{DS(ON)}$<6.5mΩ @ V_{GS}=10V
- Extremely low switching loss
- Surface-mounted package
- High UIS and UIS 100% Test
- RoHS Compliant



PDFN 5x6

Not to Scale



Ordering Information

Part Number	Package	Marking
RS100N85G	PDFN 5X6	RS100N85G

Absolute Maximun Ratings Tc=25℃ unless otherwise specified

Symbol	Parameter	RS100N85G	Units
VDSS	Drain-to-Source Voltage	100	V
ID	Continuous Drain Current（Tc=25℃）	85	A
	Continuous Drain Current Tc=100℃	55	
IDM	Pulsed Drain Current (Note*1)	316	
PD	Power Dissipation（Tc=25℃）	76	W
VGS	Gate-to-Source Voltage	±20	V
EAS	Single Pulse Avalanche Engergy (Note*2)	108	mJ
TL TPKG	Maximum Temperature for Soldering Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	300 260	℃
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

*Drain Current Limited by Maximum Junction Temperature

Caution:Stresses greater than those listed in the“Absolute Maximum Ratings”Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS100N85G	Units	Test Conditions
RθJC	Junction-to-Case	1.65	℃/W	Drain lead soldered to water cooled heatsink,PD adjusted for a peak junction temperature of +150℃.

OFF Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain-to-source Breakdown Voltage	100	--	--	V	VGS=0V,ID=250μA
IDSS	Drain-to-Source Leakage Current	--	--	1	μA	VDS=80V,VGS=0V
IGSS	Gate-to-Source Forward Leakage	--	--	100	nA	VGS=+20V ,VDS=0V
	Gate-to-Source Reverse Leakage	--	--	-100		VGS=-20V ,VDS=0V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain-to-Source On-Resistance	--	5.8	6.5	mΩ	VGS=10V,ID=20A
VGS(TH)	Gate Threshold Voltage	1.2	--	2.5	V	VGS=VDS,ID=250μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn-on Delay Time	--	16	--	nS	VDS=50V ID=20A VGS=10V RG=3Ω
trise	Rise Time	--	6	--		
td(OFF)	Turn-OFF Delay Time	--	45	--		
tfall	Fall Time	--	22	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	2362	--	pF	VGS=0V VDS=50V f=100KHz
Coss	Output Capacitance	--	743	--		
Crss	Reverse Transfer Capacitance	--	78	--		
Qg	Total Gate Charge	--	42.2	--	nC	VDS=50V ID=20A VGS=10V
Qgs	Gate-to-Source Charge	--	13	--		
Qgd	Gate-to-Drain("Miller"）Charge	--	10	--		

Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_{SD}	Source-Drain Current(Body Diode)	--	85	--	A	
I_{SDM}	Pulsed Source-Drain Current(Body Diode)		600	--	A	
V_{SD}	Diode Forward Voltage	--	--	1.2	V	IS=20A,VGS=0V
trr	Reverse Recovery Time	--	61	--	nS	VGS=0V I_F=20A,di/dt=100A/μ S
Qrr	Reverse Recovery Charge	--	88	--	nC	

Notes:

*1.Repetitive Rating: Pulse width limited by maximum junction temperature
*2.E_{AS} condition:T_J=25℃,L=0.5mH,VDS=50V

Typical Feature curve

Figure 1. Output Characteristics

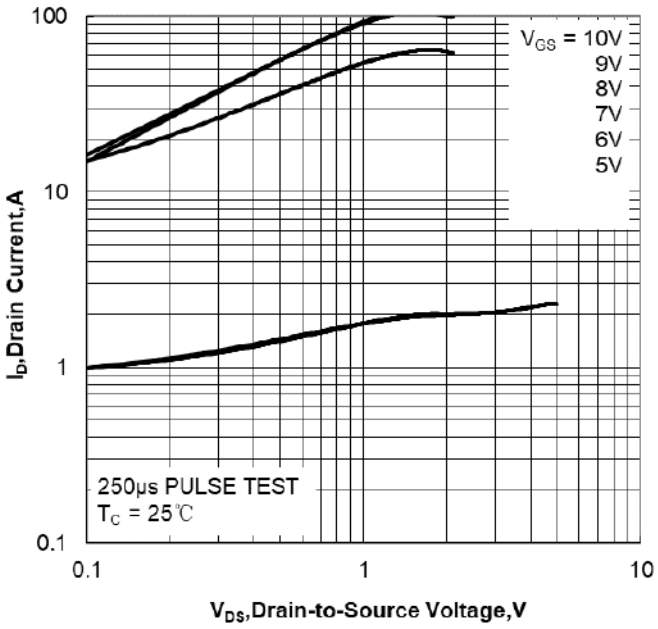


Figure 2. Transfer Characteristics

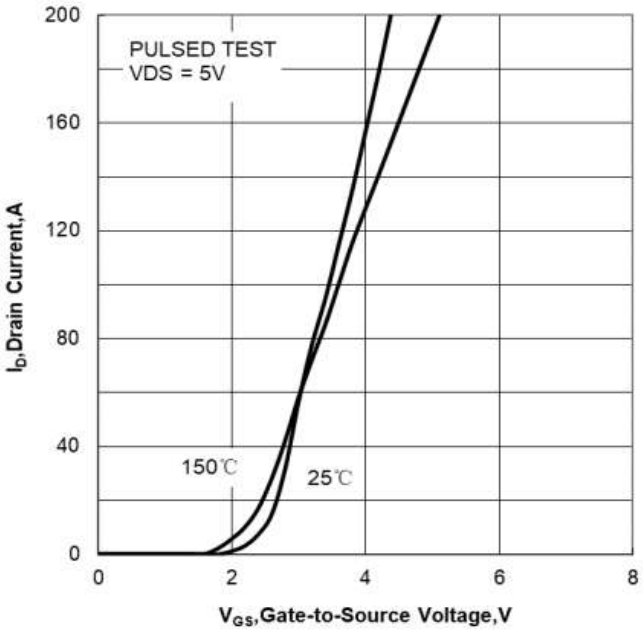


Figure 3. Drain-to-Source On Resistance vs Drain Current

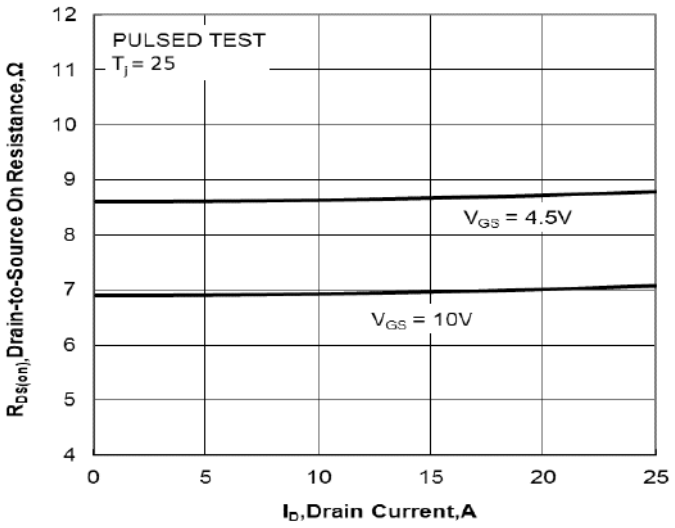


Figure 4.Body Diode Forward Voltage vs Source Current and Temperature

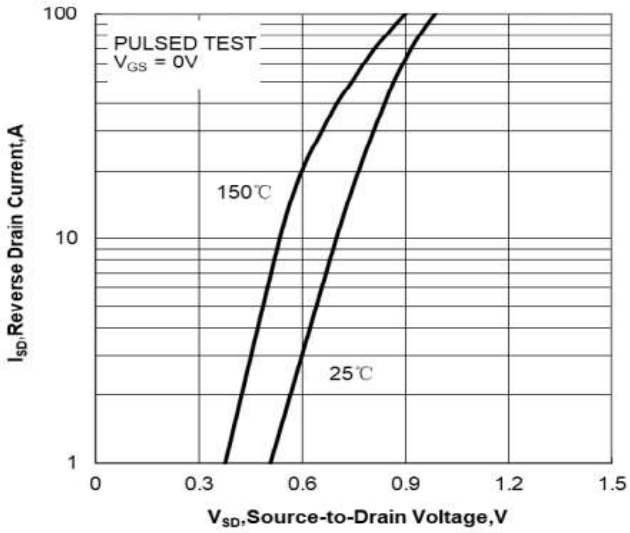


Figure 5. Capacitance Characteristics

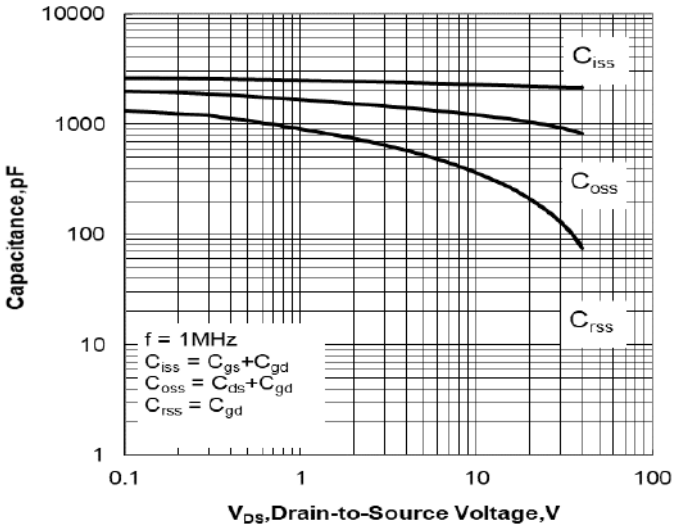


Figure 6. Gate Charge Characteristics

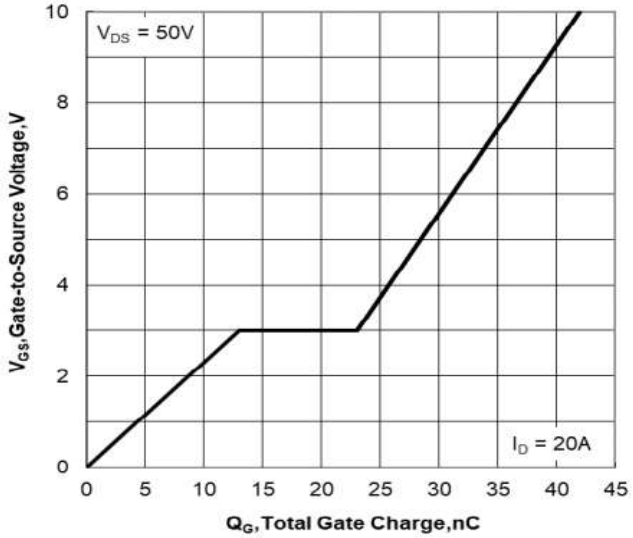


Figure 7. Normalized Breakdown Voltage vs Junction Temperature

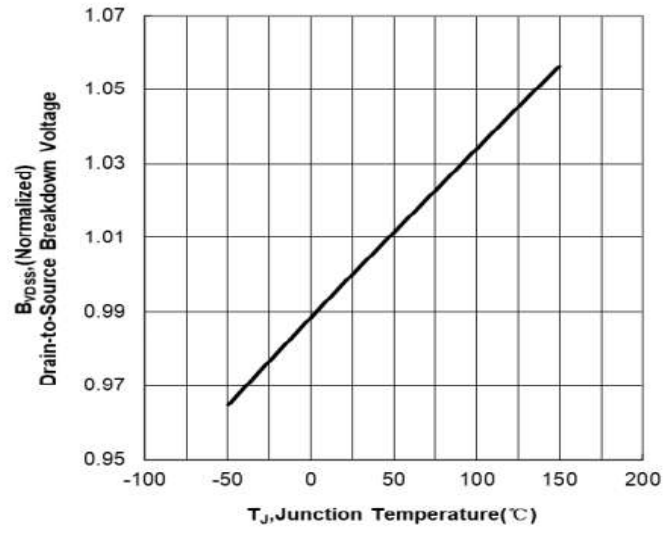


Figure 8. Normalized On Resistancevs Junction Temperature

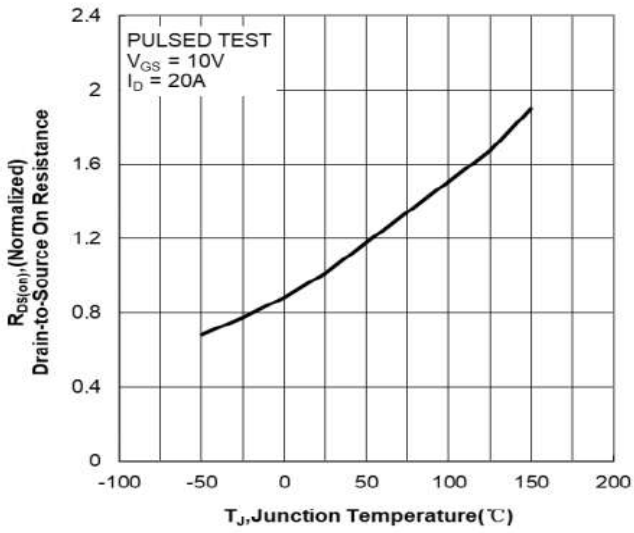


Figure 9. Maximum Continuous Drain Current vs Case Temperature

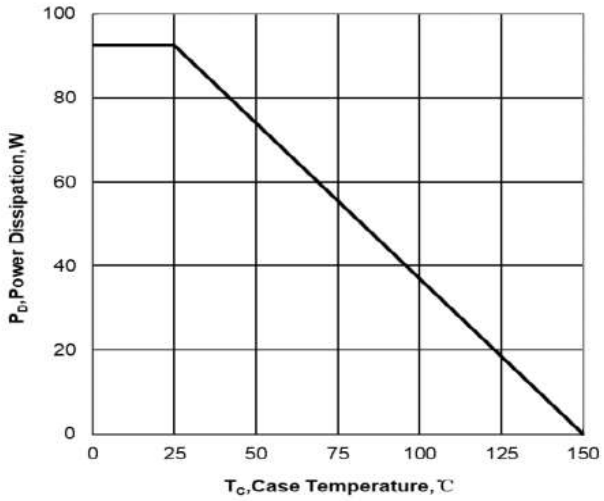


Figure 10. Maximum Power Dissipation vs Case Temperature

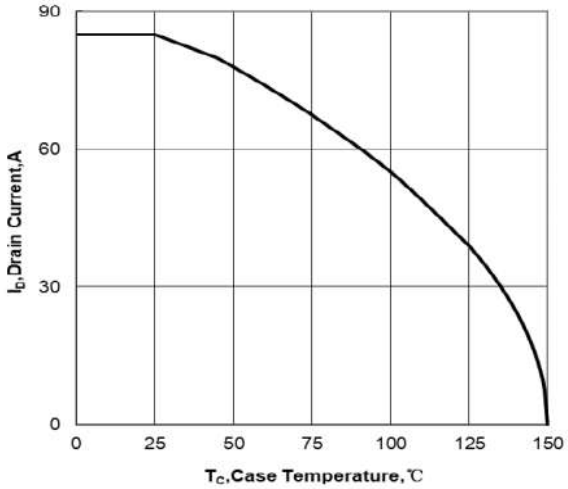


Figure11. Drain-to-Source On Resistancevs Gate Voltage and Drain Current

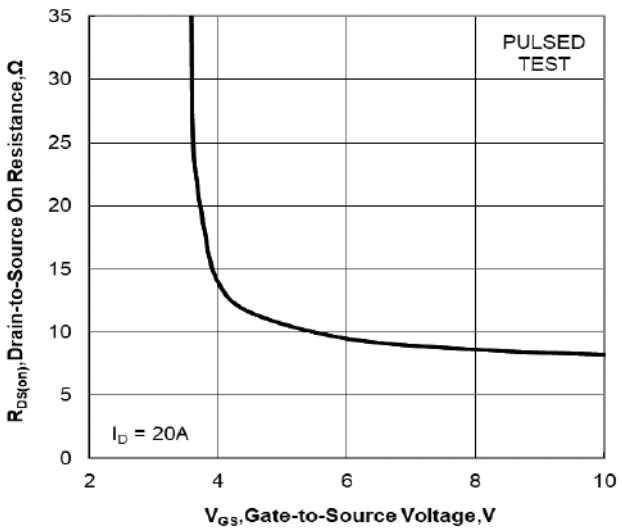


Figure 12. Maximum Safe Operating Area

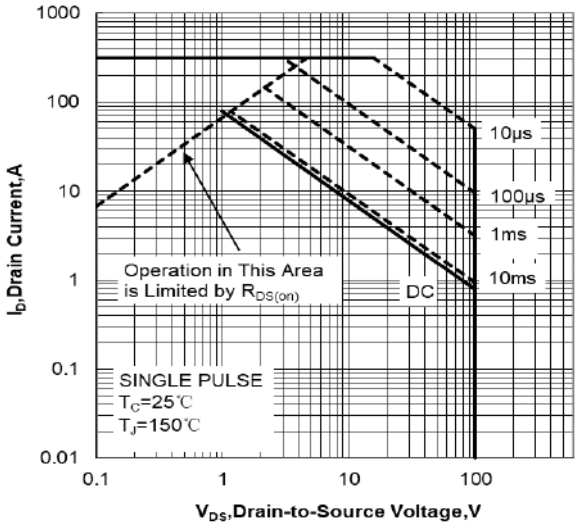
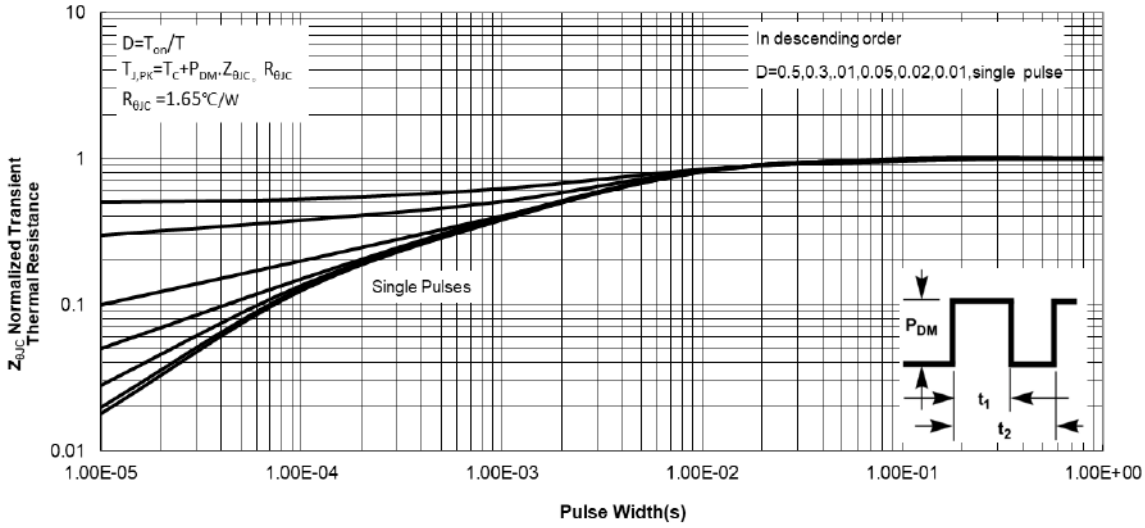


Figure 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case



Test Circuits and Waveforms

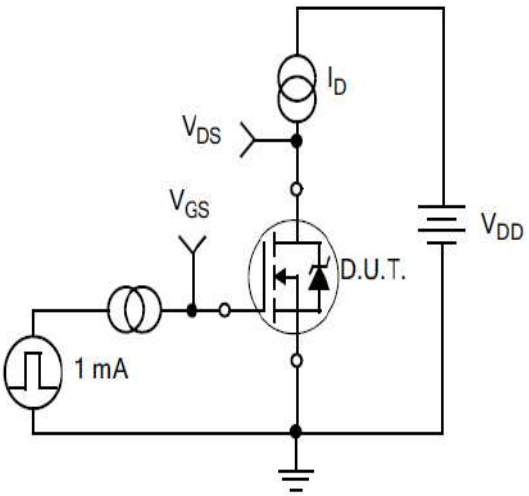


Figure A.
Gate Charge Test Circuit

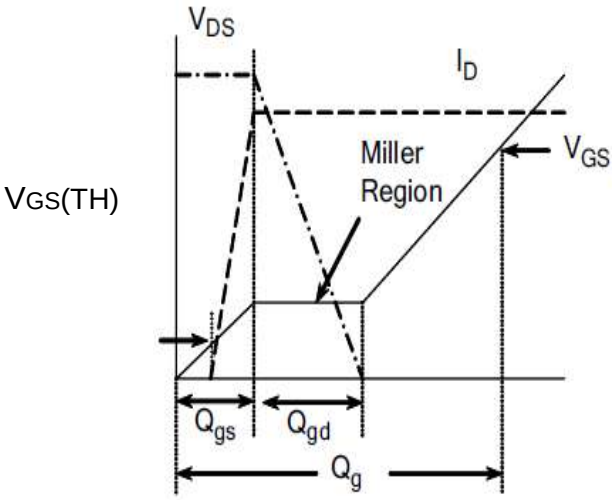


Figure B.
Gate Charge Waveform

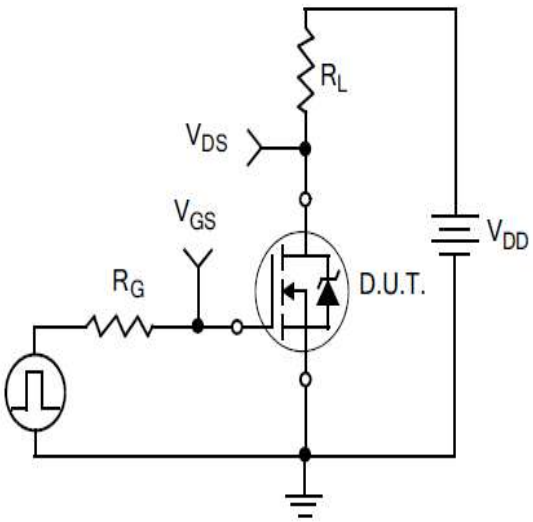


Figure C.
Resistive Switching Test Circuit

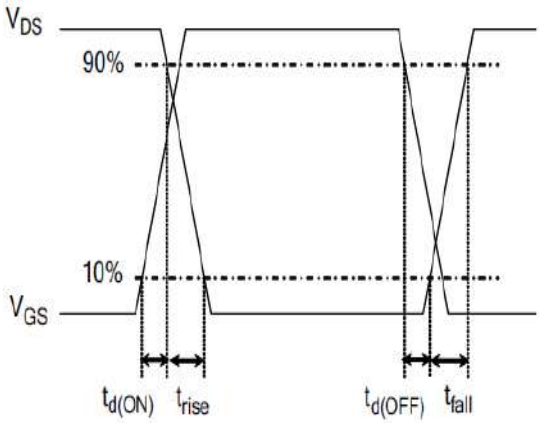


Figure D.
Resistive Switching Waveforms

Test Circuits and Waveforms

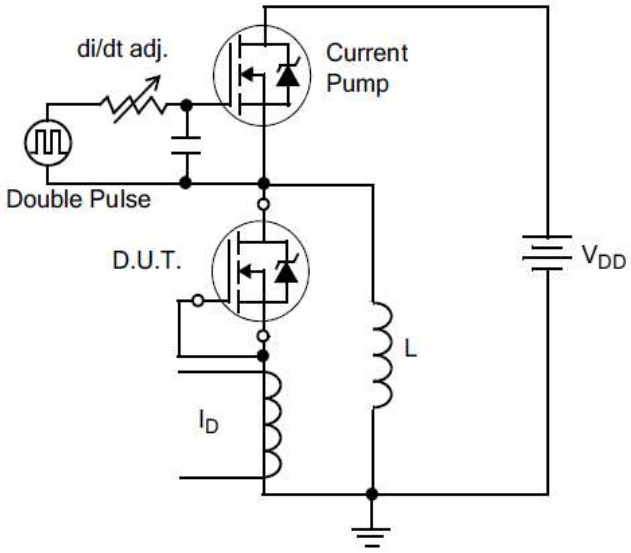


Figure E.Diode Reverse Recovery Test Circuit

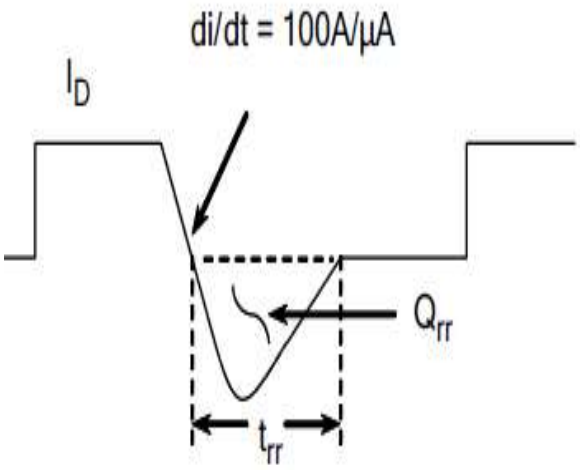


Figure F.Diode Reverse Recovery Waveform

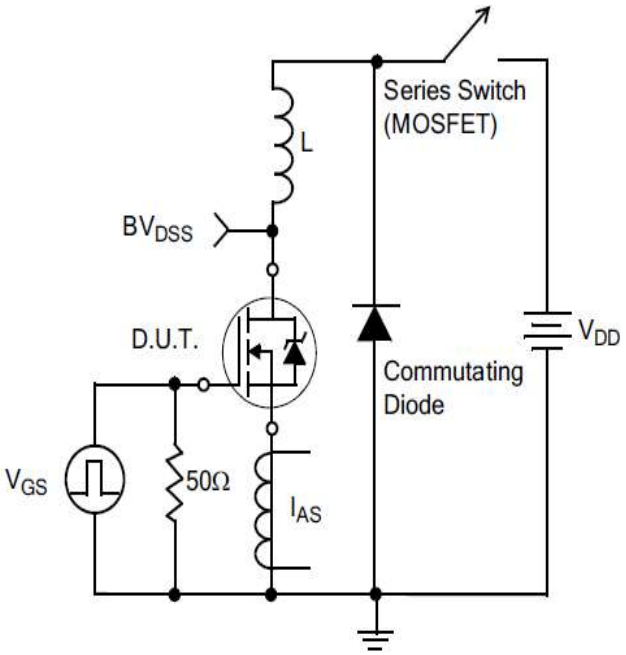
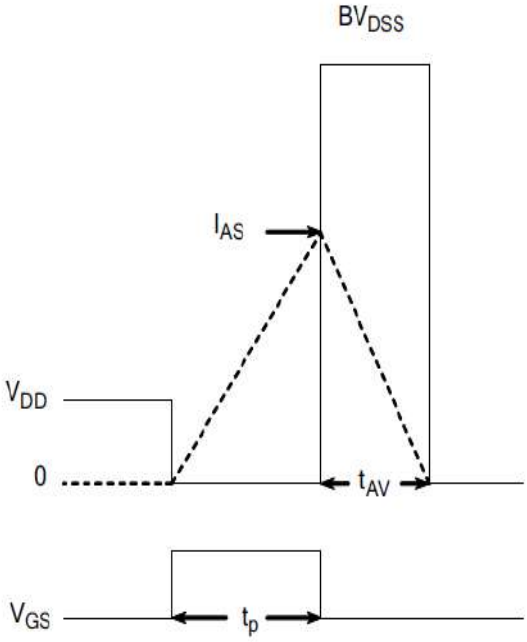


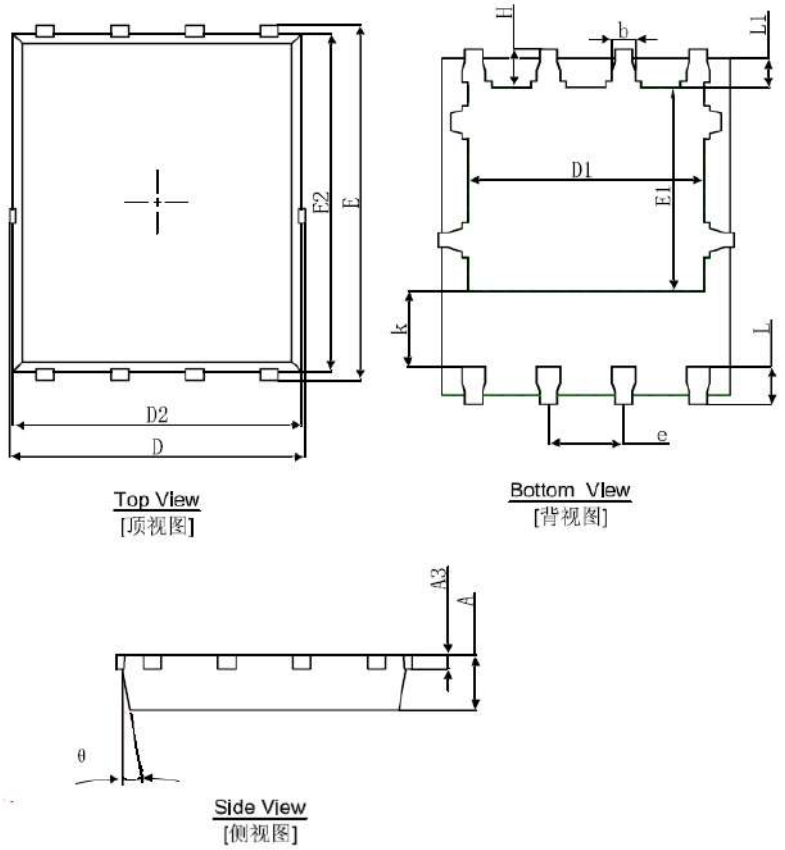
Figure G.Unclamped Inductive Switching Test Circuit



$$E_{AS}= \frac{I_{AS}^2 L}{2}$$

Figure H.Unclamped Inductive Switching Waveforms

PDFN5X6-8L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	8°	12°	8°	12°

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