N Channel MOSFET

Lead Free Package and Finish

Applications:

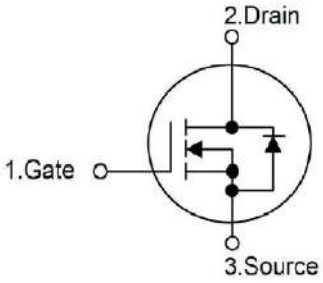
- Adapter & Charger
- SMPS Standby Power
- AC-DC Switching Power Supply
- LED driving power

I_D	$R_{DS(ON)}$(Typ.)	V_{DSS}
18A	0.28Ω	500V

Features:

- Low On Resistance
- Low Gate Charge
- Peak Current vs Pulse Width Curve
- RoHS Compliant

Not to Scale



Ordering Information

Part Number	Package	Marking
RS18N50F	TO-220F	RS18N50F

Absolute Maximun Ratings Tc=25℃ unless otherwise specified

Symbol	Parameter	RS18N50F	Units
V_{DSS}	Drain-to-Source Voltage (Note*1)	500	V
I_D	Continuous Drain Current	18.0	A
I_D@ 100 ℃	Continuous Drain Current	10.6	
I_{DM}	Pulsed Drain Current (Note*2)	72.0	
P_D	Power Dissipation	98	W
V_{GS}	Gate-to-Source Voltage	±30	V
EAS	Single Pulse Avalanche Engergy L=10mH VDD=50V RG=25Ω Starting TJ=25℃ (Note*2)	1280	mJ
IAS		16	A
EAR	Repetitive Avalanche Energy	89	mJ
TL	Maximum Temperature for Soldering Leads at 0.063in(1.6mm)from Case for 10 seconds	300	℃
TPKG	Package Body for 10 seconds	260	
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

*Drain Current Limited by Maximum Junction Temperature

Caution:Stresses greater than those listed in the"Absolute Maximum Ratings"Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS18N50F	Units	Test Conditions
$R_{\theta JC}$	Junction-to-Case	1.27	℃/W	Drain lead soldered to water cooled heatsink,P_D adjusted for a peak junction temperature of +150℃.
$R_{\theta JA}$	Junction-to-Ambient	60		1 cubic foot chamber,free air.

Static Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-source Breakdown Voltage	500	--	--	V	V_{GS}=0V,I_D=250μA
I_{DSS}	Drain-to-Source Leakage Current	--	--	1.0	μA	V_{DS}=500V,VGS=0V
I_{GSS}	Gate-to-Source Forward Leakage	--	--	100	nA	V_{GS}=+30V V_{DS}=0V
	Gate-to-Source Reverse Leakage	--	--	-100		V_{GS}=-30V V_{DS}=0V

Static Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{DS(on)}$	Static Drain-to-Source On-Resistance (Note*3)	--	0.28	0.33	Ω	V_{GS}=10V,I_D=9A
$V_{GS(TH)}$	Gate Threshold Voltage	2.0	--	4.0	V	V_{GS}=V_{DS},I_D=250μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	35	--	nS	V_{DS}=250V I_D=18A R_G=25Ω
t_{rise}	Rise Time	--	50	--		
$t_{d(OFF)}$	Turn-OFF Delay Time	--	180	--		
t_{fall}	Fall Time	--	65	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
C_{iss}	Input Capacitance	--	2148	--	pF	V_{GS}=0V V_{DS}=25V f=1.0MHz
C_{oss}	Output Capacitance	--	252	--		
C_{rss}	Reverse Transfer Capacitance	--	22	--		
Q_g	Total Gate Charge	--	58.4	--	nC	V_{DS}=400V I_D=18A V_{GS}=10V (Note:3,4)
Q_{gs}	Gate-to-Source Charge	--	10.2	--		
Q_{gd}	Gate-to-Drain("Miller"）Charge	--	22.1	--		

Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current	--	--	18.0	A	Integral pn-diode in MOSFET
I_{SM}	Maximum Pulsed Current	--	--	72.0	A	
V_{SD}	Diode Forward Voltage	--	--	1.4	V	IS=10A,VGS=0V
t_{rr}	Reverse Recovery Time	--	430	--	nS	VGS=0V IS=18A,di/dt=100A/μs
Q_{rr}	Reverse Recovery Charge	--	6.5	--	μC	

Notes:

*1.TJ=±25℃ to +150℃.
*2.Repetitive rating;pulse width limited by maximum junction temperature.
*3.Pulse width≤300μs;duty cycle ≤1%.

Typical Feature curve T_J = 25ºC, unless otherwise noted

Figure 1. Output Characteristics (TJ = 25ºC)

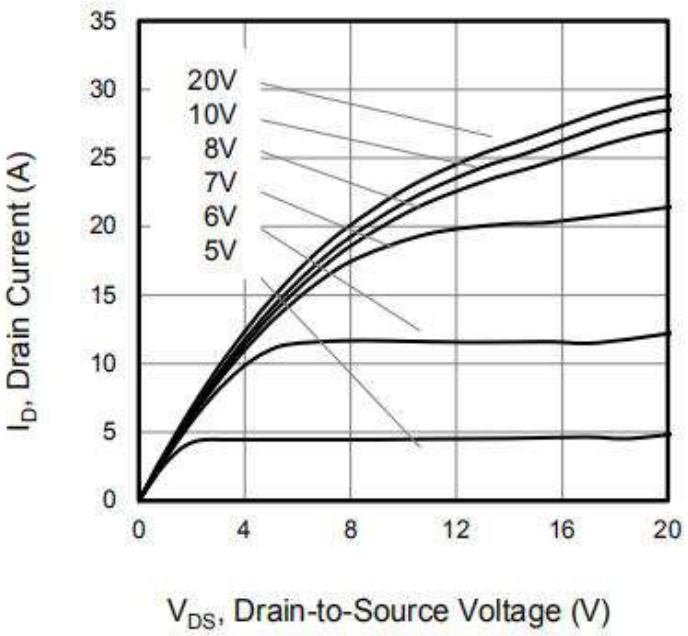


Figure2. Body Diode Forward Voltage

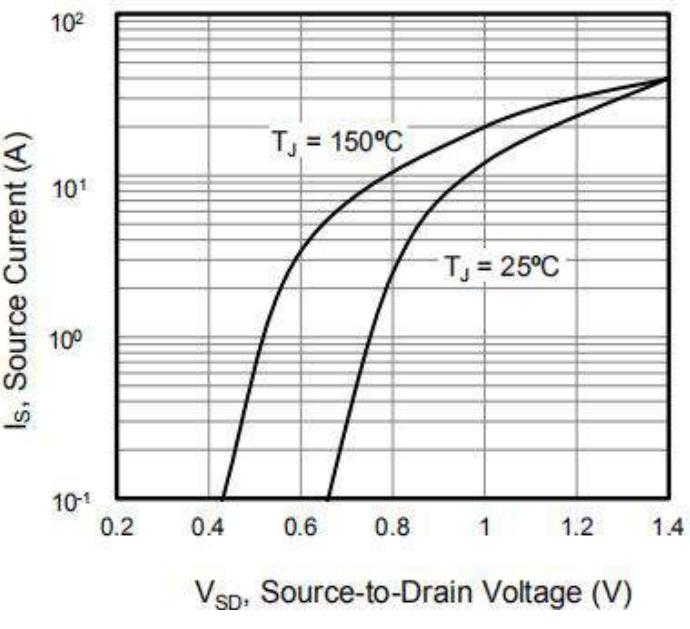


Figure 3. Drain Current vs. Temperature

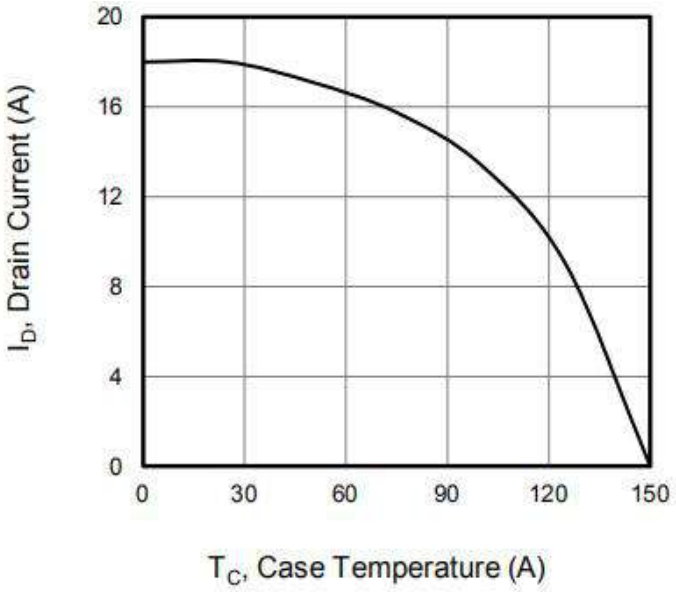


Figure 4. BVDSS Variation vs. Temperature

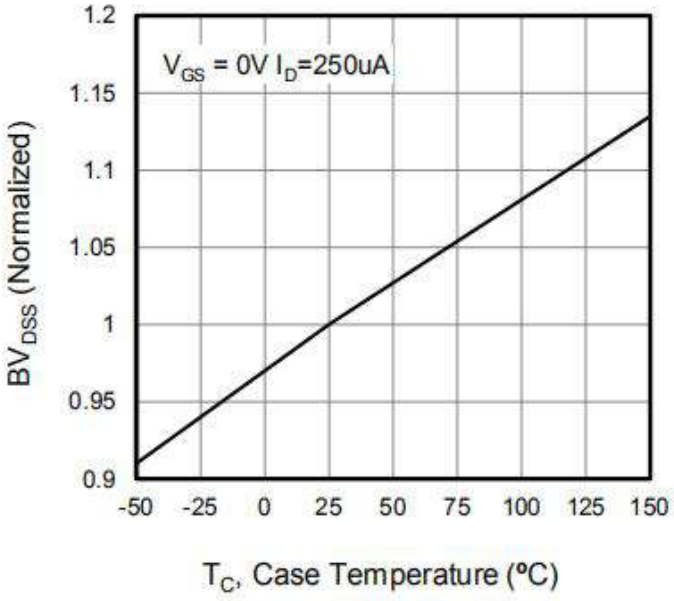


Figure 5. Transfer Characteristics

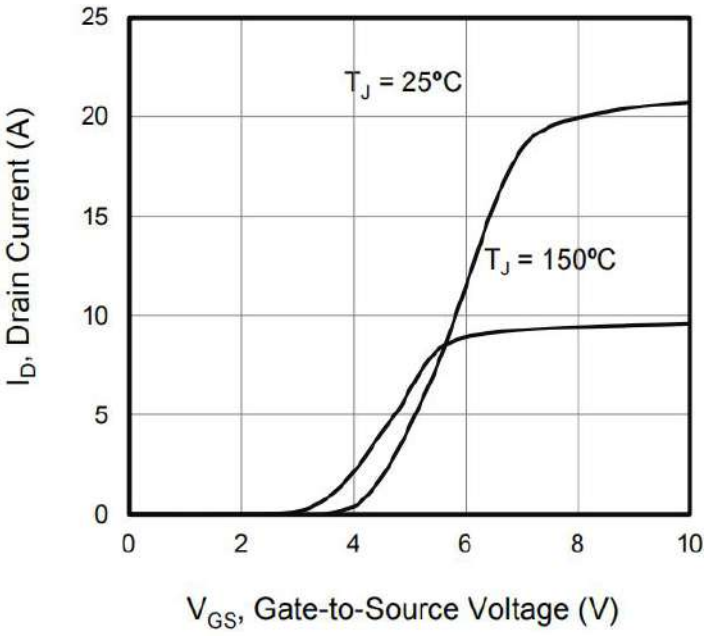


Figure 6. On-Resistance vs. Temperature

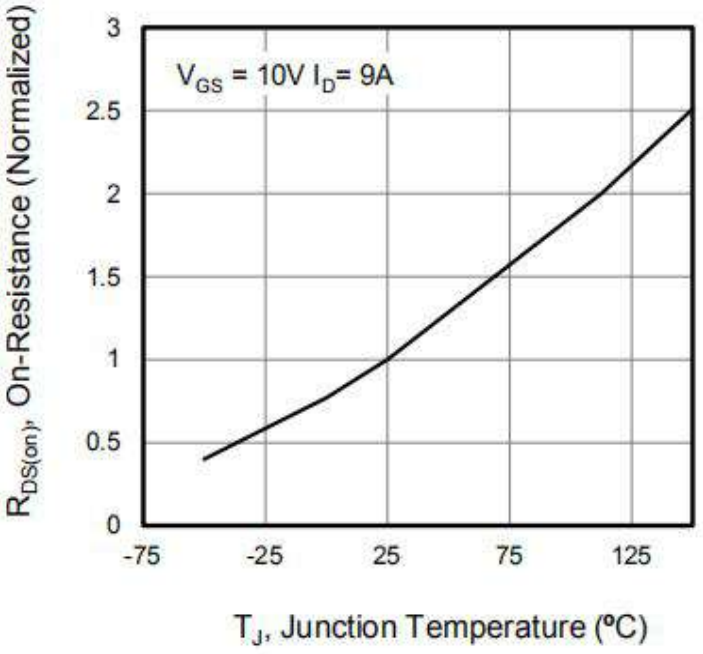


Figure 7. Capacitance

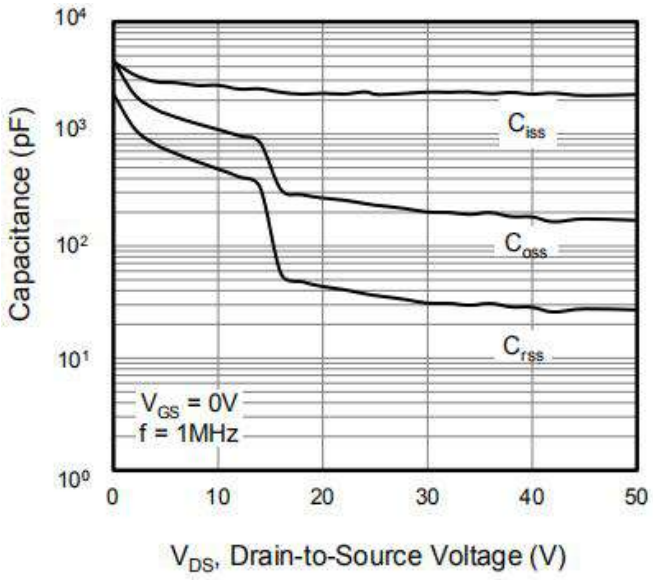


Figure 8. Gate Charge

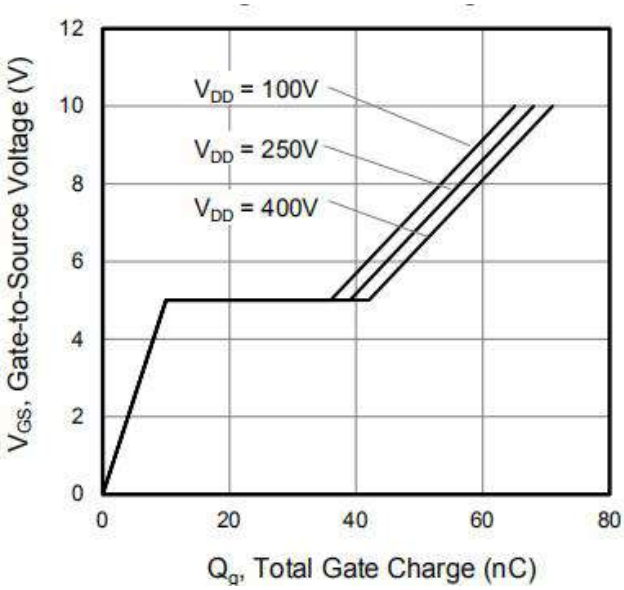
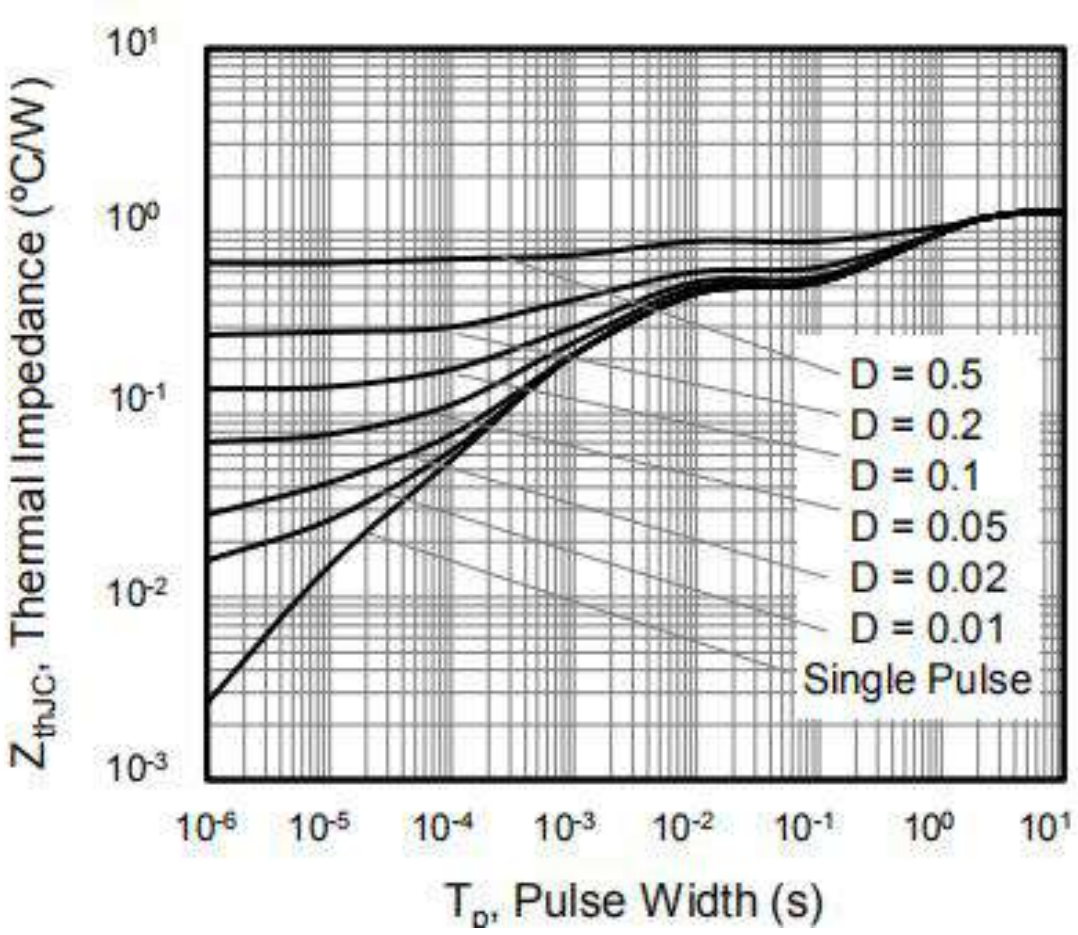


Figure 9. Transient Thermal Impedance
TO-220F



Test Circuits and Waveforms

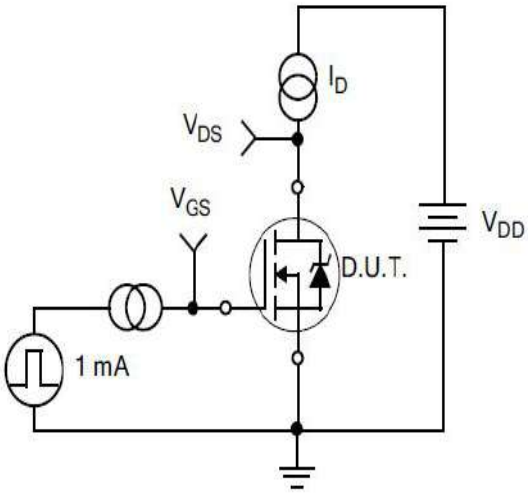


Figure10.
Gate Charge Test Circuit

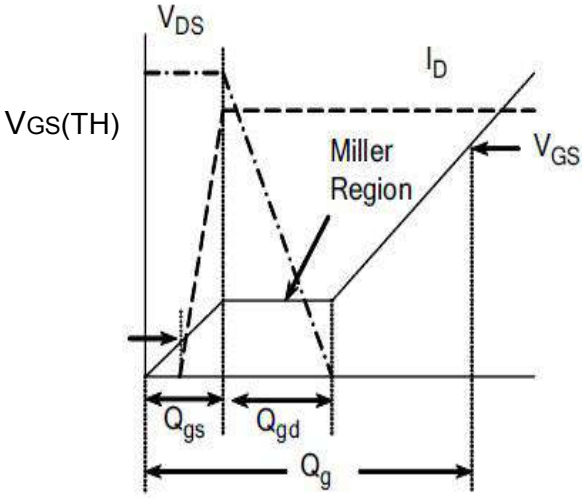


Figure11.
Gate Charge Waveform

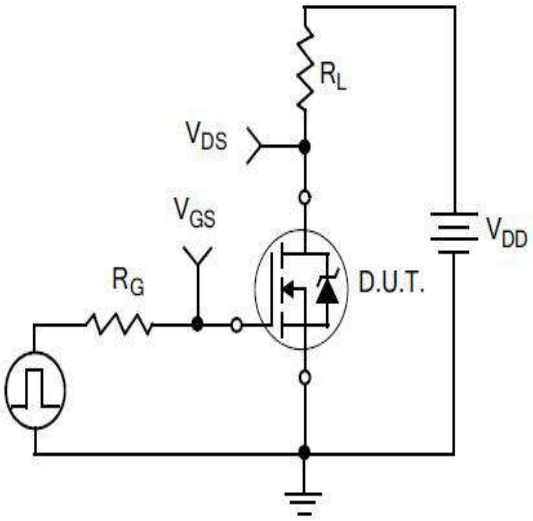


Figure12.
Resistive Switching Test Circuit

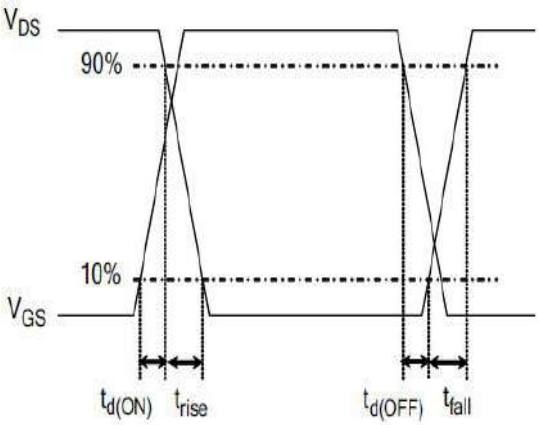


Figure13.
Resistive Switching Waveforms

Test Circuits and Waveforms

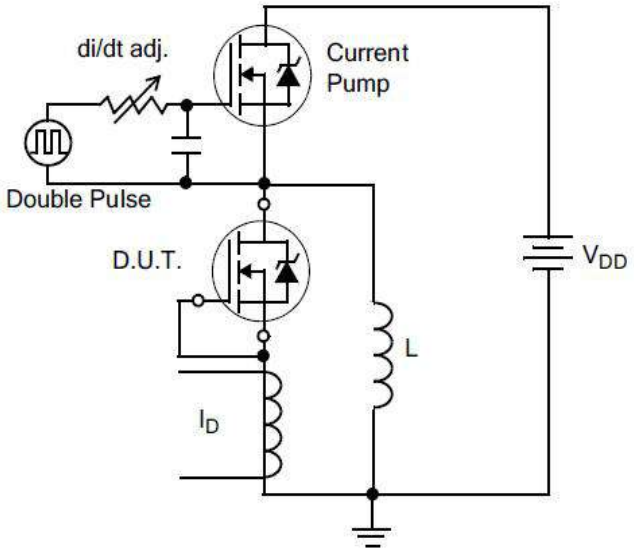


Figure14.Diode Reverse Recovery Test Circuit

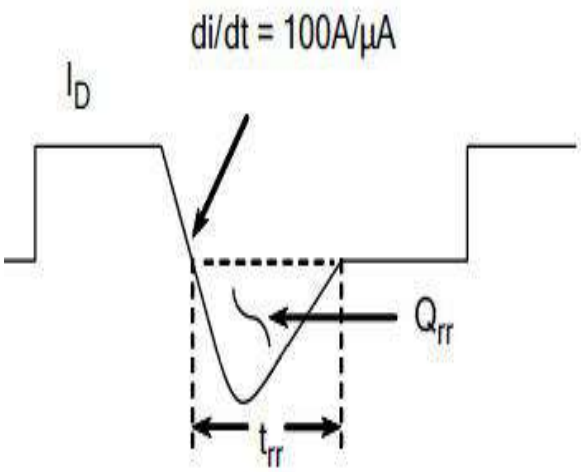


Figure15.Diode Reverse Recovery Waveform

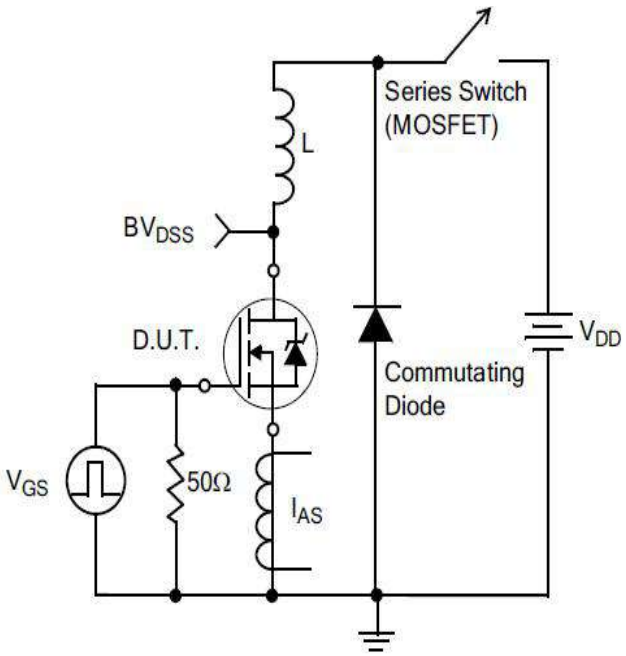
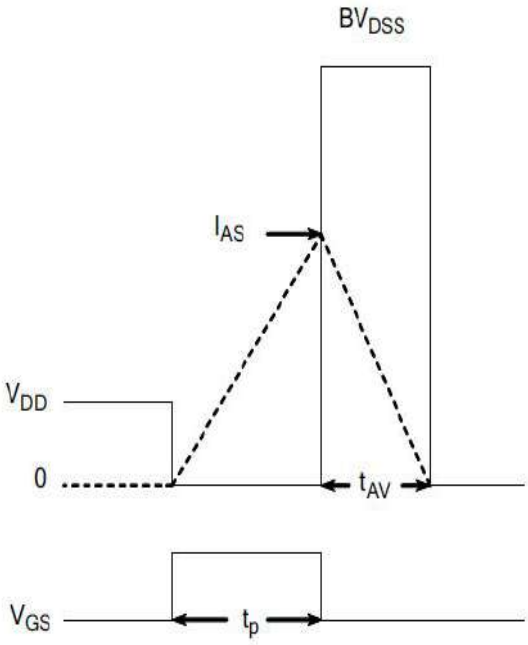


Figure16.Unclamped Inductive Switching Test Circuit



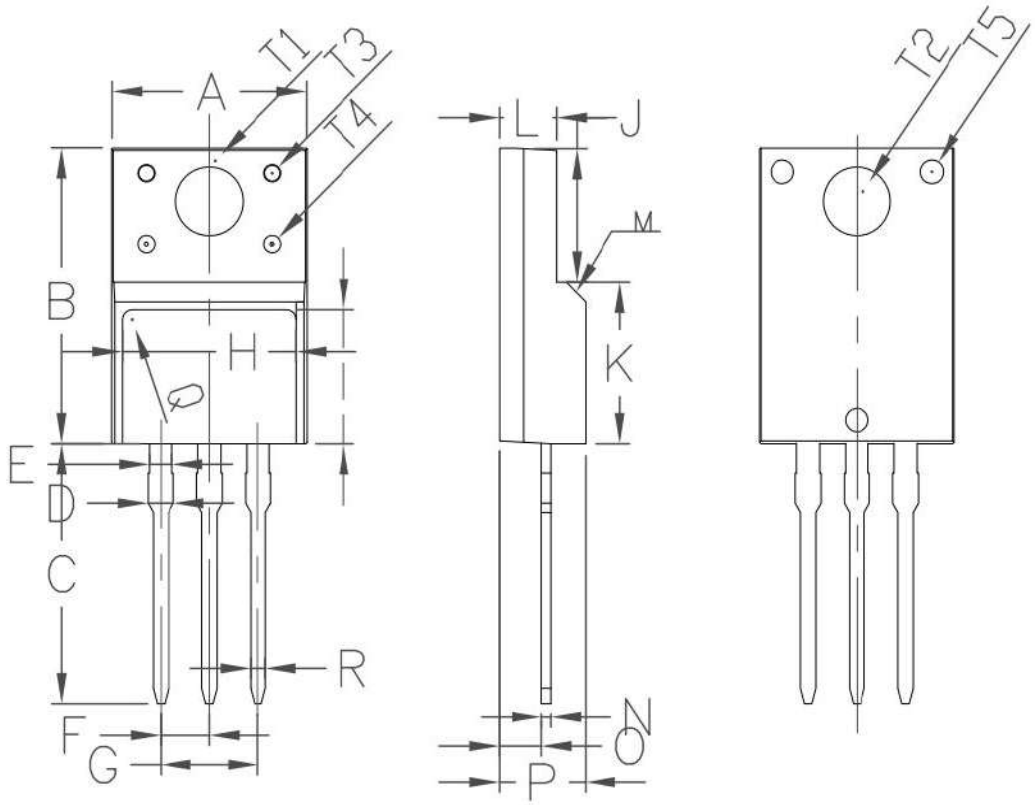
$$E_{AS}=\frac{I_{AS}^2 L}{2}$$

Figure17.Unclamped Inductive Switching Waveforms

Package outline drawing

TO-220F

Unit: mm



Symbol	Min	Non	Max
A	9.96	10.16	10.36
B	15.67	15.87	16.07
C	13.14	13.34	13.54
D	1.20	1.30	1.40
E		1.20	
F		2.54	
G		5.08	
H	7.60	7.80	8.00
I	7.10	7.30	7.50
J	6.48	6.68	6.88
K	8.99	9.19	9.39
L	2.34	2.54	2.74
M		45°	
N	0.49	0.50	0.52
O	2.15	2.35	2.55
P	4.50	4.70	4.90
Q		0.50	
S	4°	4.5°	5°
T1		3.45	
T2		3.18	
T3		1.50	
T4		1.20	
T5		1.50	
R	0.77	0.8	0.83

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