RS4N70F

N Channel MOSFET

Lead Free Package and Finish

Applications:

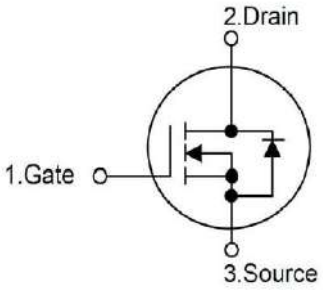
- •Adapter & Charger
- •SMPS Standby Power
- •AC-DC Switching Power Supply
- •LED driving power

I_D	$R_{DS(ON)}$(Typ.)	V_{DSS}
4.0A	2.5Ω	700V

Features:

- •Low On Resistance
- •Low Gate Charge
- •Peak Current vs Pulse Width Curve
- •RoHS Compliant

Not to Scale



Ordering Information

Part Number	Package	Marking
RS4N70F	TO-220F	RS4N70F

Absolute Maximun Ratings Tc=25℃ unless otherwise specified

Symbol	Parameter	RS4N70F	Units
V_{DSS}	Drain-to-Source Voltage (Note*1)	700	V
I_D	Continuous Drain Current	4.0	A
I_D@ 100 ℃	Continuous Drain Current	2.53	
I_{DM}	Pulsed Drain Current (Note*2)	16.0	
P_D	Power Dissipation	36	W
	Derating Factor above 25℃	0.26	W/℃
V_{GS}	Gate-to-Source Voltage	±30	V
E_{AS}	Single Pulse Avalanche Engergy I_{AS}=4A V_{DD}=50V R_G=25Ω Starting T_J=25℃	242	mJ
T_L	Maximum Temperature for Soldering	300	℃
T_{PKG}	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	260	
T_J and T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	

*Drain Current Limited by Maximum Junction Temperature

Caution:Stresses greater than those listed in the“Absolute Maximum Ratings”Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS4N70F	Units	Test Conditions
$R_{\theta JC}$	Junction-to-Case	3.47	℃/W	Drain lead soldered to water cooled heatsink,P_D adjusted for a peak junction temperature of +150℃.
$R_{\theta JA}$	Junction-to-Ambient	62.5		1 cubic foot chamber,free air.

OFF Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-source Breakdown Voltage	700	--	--	V	V_{GS}=0V,I_D=250μA
I_{DSS}	Drain-to-Source Leakage Current	--	--	1.0	μA	V_{DS}=700V,V_{GS}=0V
I_{GSS}	Gate-to-Source Forward Leakage	--	--	100	nA	V_{GS}=+30V V_{DS}=0V
	Gate-to-Source Reverse Leakage	--	--	-100		V_{GS}=-30V V_{DS}=0V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	--	2.5	2.7	Ω	V_{GS}=10V,I_D=2A
$V_{GS(TH)}$	Gate Threshold Voltage	3.0	--	4.0	V	V_{GS}=V_{DS},I_D=250μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	12	--	ns	V_{DS}=350V I_D=4.0A R_G=25Ω (Note:3,4)
t_{rise}	Rise Time	--	22	--		
$t_{d(OFF)}$	Turn-OFF Delay Time	--	50	--		
t_{fall}	Fall Time	--	48	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
C_{iss}	Input Capacitance	--	580	--	pF	V_{GS}=0V V_{DS}=25V f=1.0MHz
C_{oss}	Output Capacitance	--	69.5	--		
C_{rss}	Reverse Transfer Capacitance	--	10.9	--		
Q_g	Total Gate Charge	--	15	17.5	nC	V_{DS}=560V I_D=4.0A V_{GS}=10V (Note:3,4)
Q_{gs}	Gate-to-Source Charge	--	2.5	--		
Q_{gd}	Gate-to-Drain("Miller"）Charge	--	7.5	--		

Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current	--	--	4.0	A	Integral pn-diode in MOSFET
I_{SM}	Maximum Pulsed Current	--	--	16.0	A	
V_{SD}	Diode Forward Voltage	--	--	1.4	V	I_S=4.0A,V_{GS}=0V
t_{rr}	Reverse Recovery Time	--	250	--	ns	V_{GS}=0V I_S=4.0A,di/dt=100A/μs
Q_{rr}	Reverse Recovery Charge	--	3.5	--	μC	

Notes:

*1.TJ=±25℃ to +150℃.
*2.Repetitive rating;pulse width limited by maximum junction temperature.
*3.Pulse width≤300μs;duty cycle ≤1%.
*4.Basically not affected by temperature.

Typical Feature curve TJ = 25ºC, unless otherwise noted

Figure 1. Output Characteristics (T_J = 25ºC)

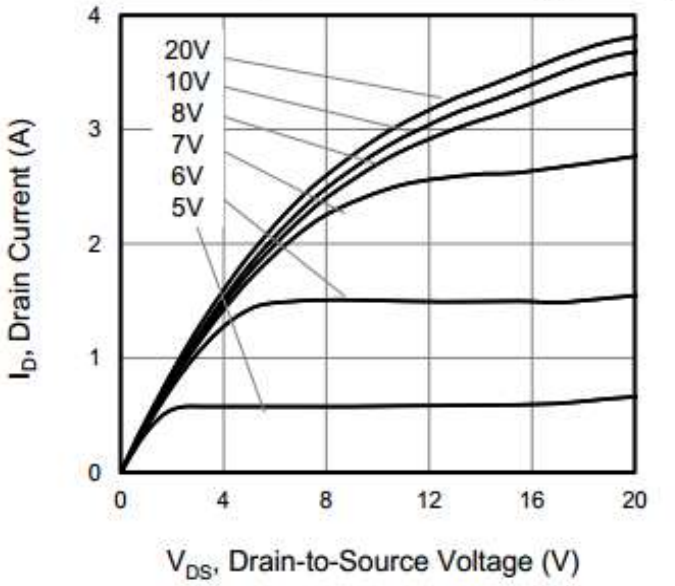


Figure 2. Body Diode Forward Voltage

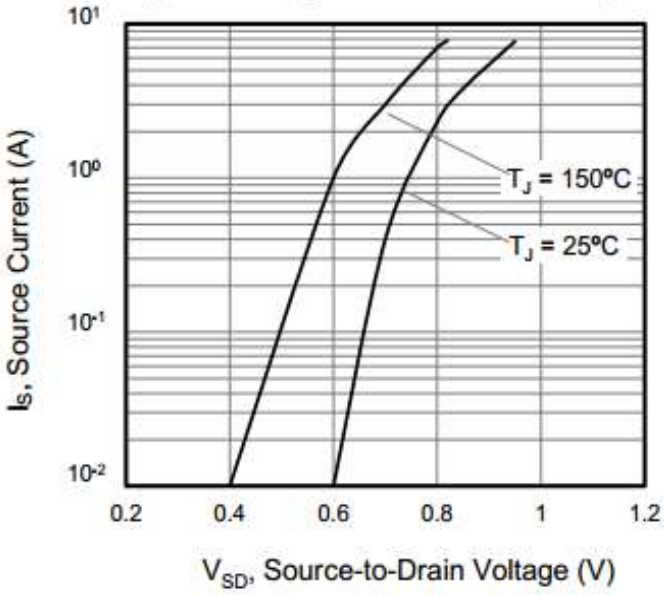


Figure 3. Drain Current vs. Temperature

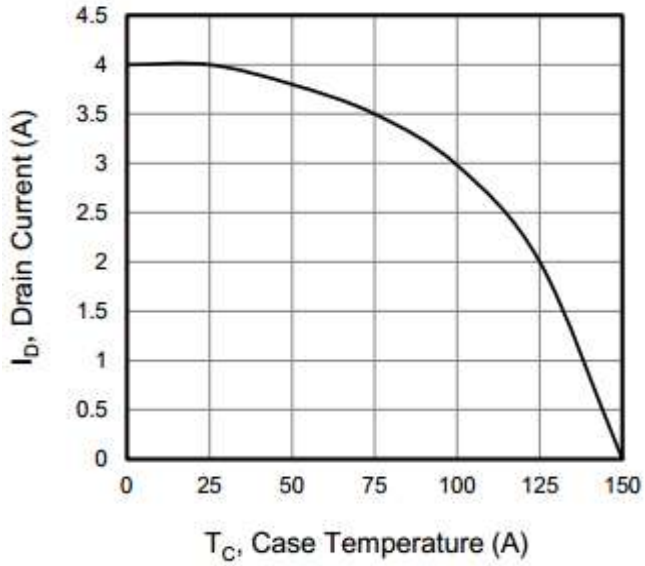


Figure 4. Power Dissipation vs. Temperature

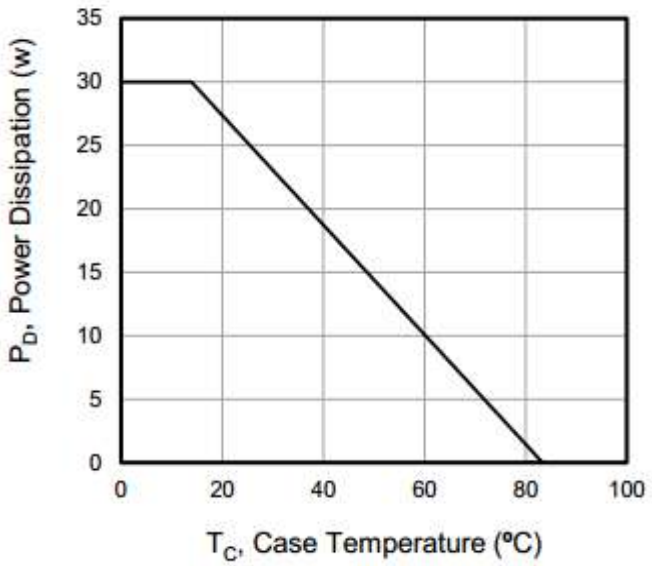


Figure 5. Transfer Characteristics

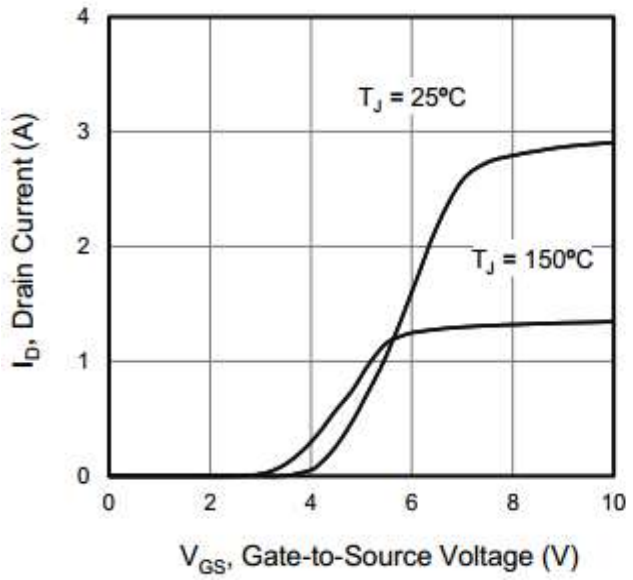


Figure 6. On-Resistance vs. Temperature

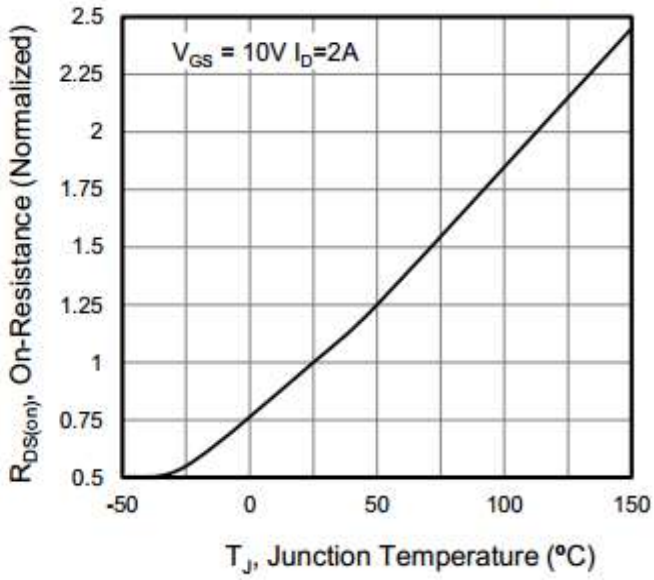


Figure 7. Capacitance

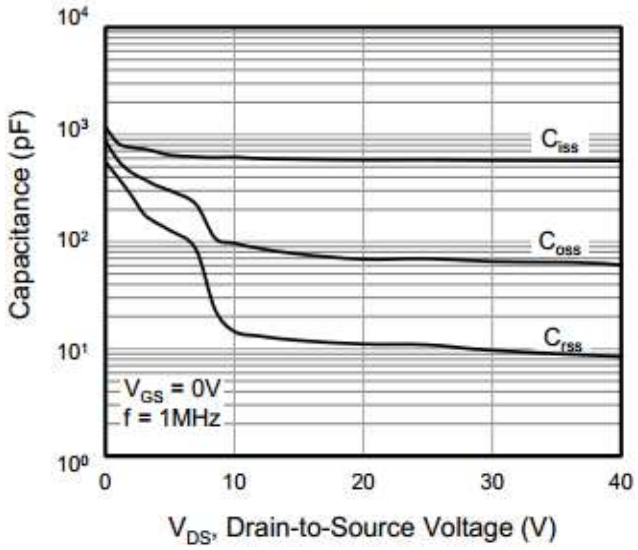


Figure 8. Gate Charge

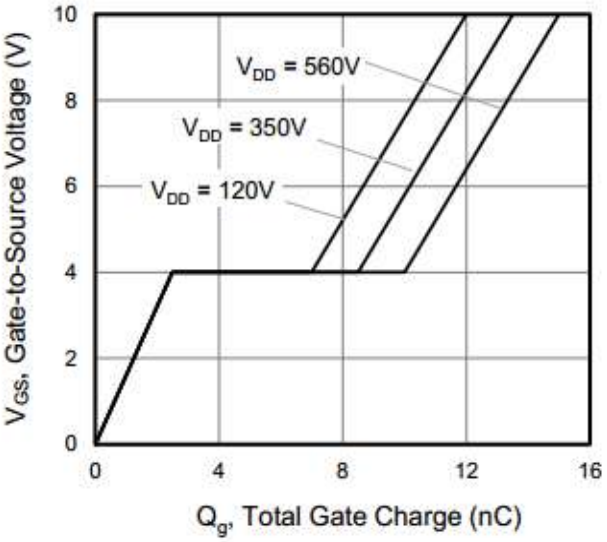
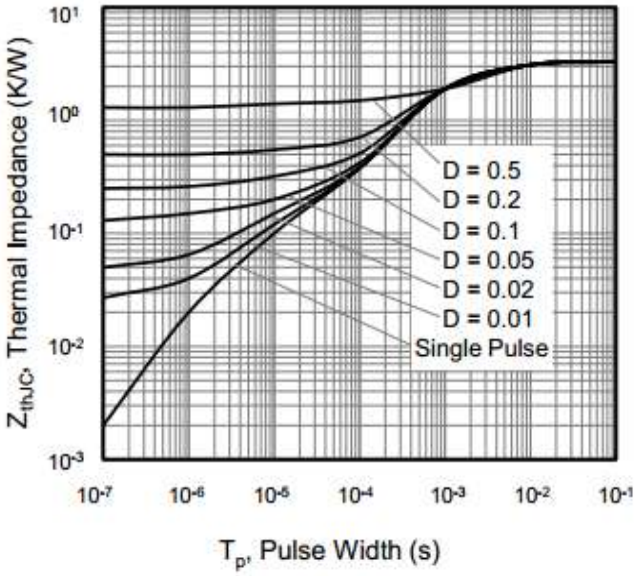


Figure 9. Transient Thermal Impedance
TO-220F



Test Circuits and Waveforms

Figure10.
Gate Charge Test Circuit

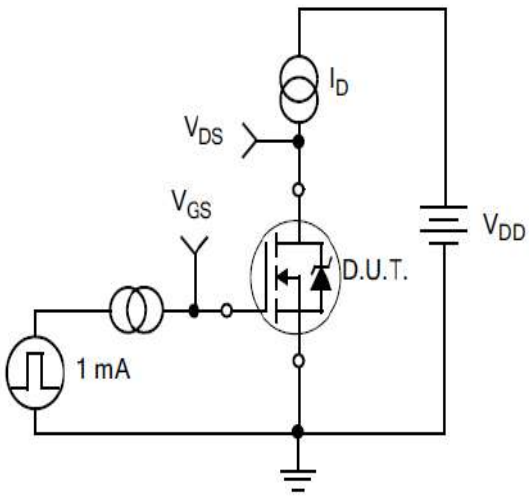


Figure11.
Gate Charge Waveform

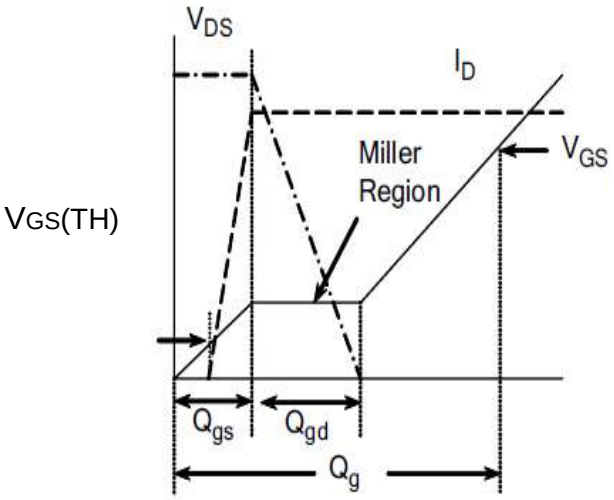


Figure12.
Resistive Switching Test Circuit

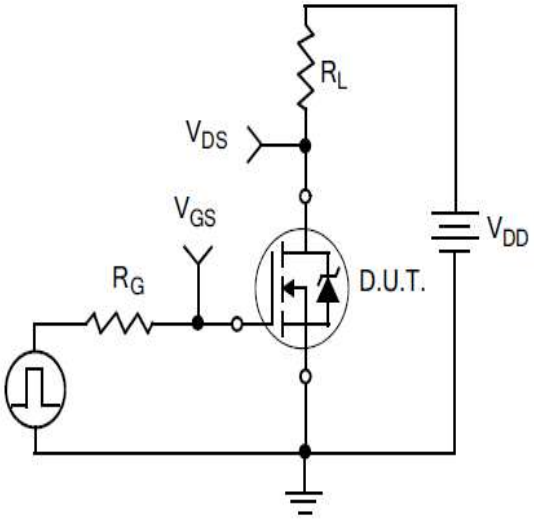
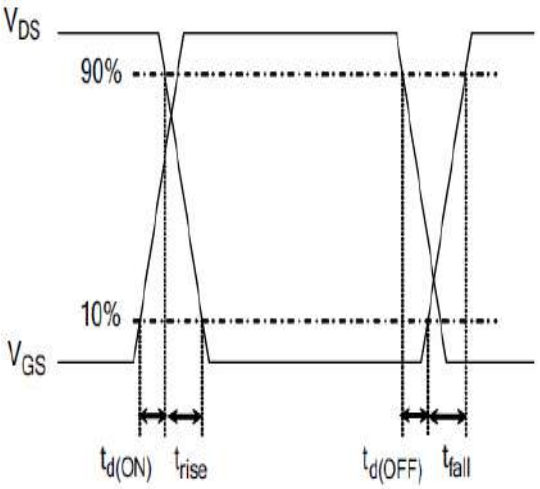


Figure13.
Resistive Switching Waveforms



Test Circuits and Waveforms

Figure14.Diode Reverse Recovery Test Circuit

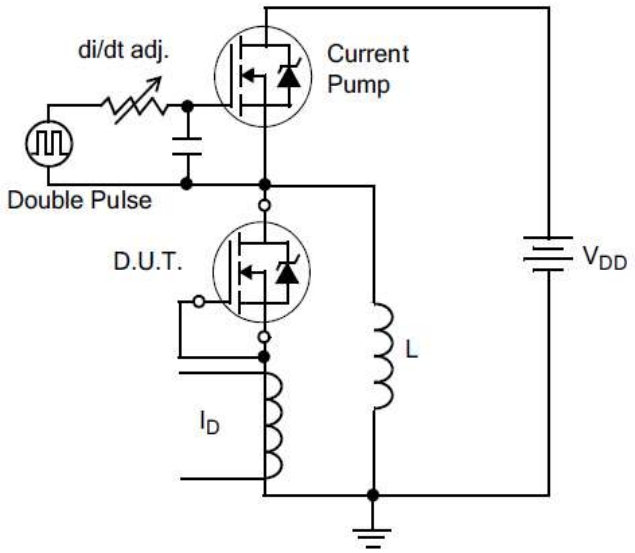


Figure15.Diode Reverse Recovery Waveform

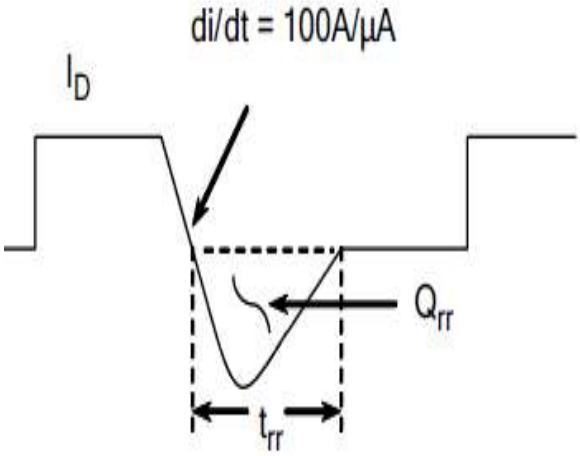


Figure16.Unclamped Inductive Switching Test Circuit

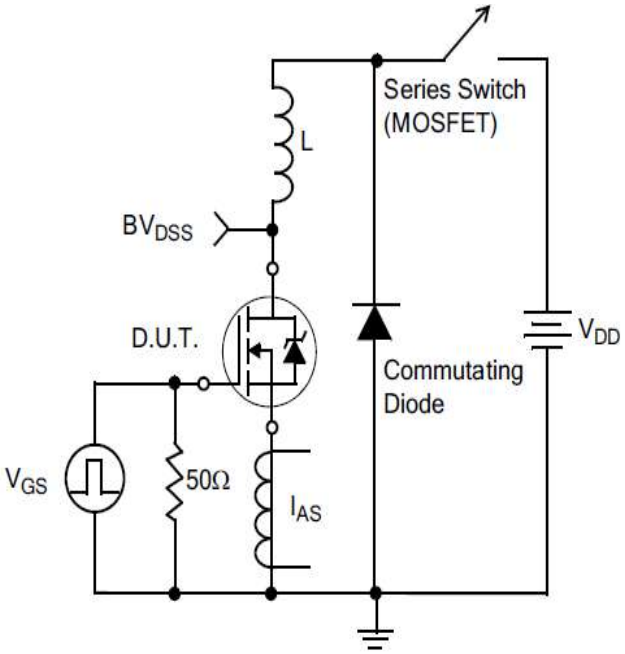
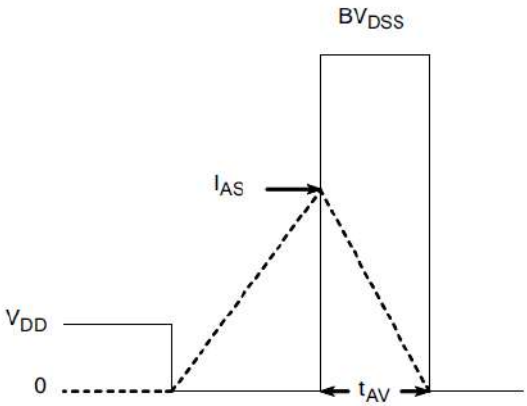


Figure17.Unclamped Inductive Switching Waveforms

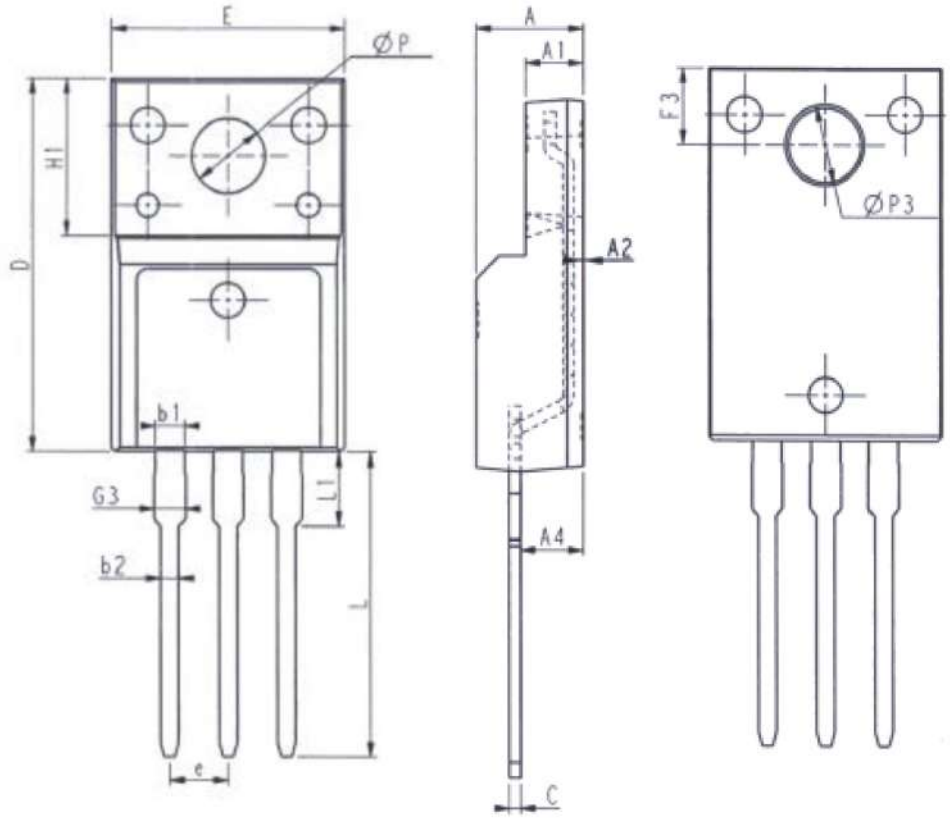


$$E_{AS}=\frac{I_{AS}^2 L}{2}$$

Package outline drawing

Unit：mm

TO-220F



Unit: mm		
Symbol	Min.	Max.
E	9.96	10.36
A	4.50	4.90
A1	2.34	2.74
A2	0.30	0.60
A4	2.56	2.96
c	0.40	0.65
D	15.57	16.17
H1	6.70REF	
e	2.54BSC	

Unit: mm		
Symbol	Min.	Max.
L	12.68	13.28
L1	2.93	3.13
P	3.03	3.38
P3	3.15	3.65
F3	3.15	3.45
G3	1.25	1.55
b1	1.18	1.43
b2	0.70	0.95

Disclaimers:

Reasunos Semiconductor Technology CO.,LTD(Reasunos)reserves the right to make changes without notice in order to improve reliability,function or design and to discontinue any product or service without notice .Customers should obtain the latest relevant information before orders and should verify that such information in current and complete.All products are sold subject to Reasunos's terms and conditions supplied at the time of order acknowledgement.

Reasunos Semiconductor Technology CO.,LTD warrants performance of its hardware products to the speciffications at the time of sale.Testing,reliability and quality control are used to the extene Reasunos deems necessary to support this warrantee. Except where agreed upon by contr-actual agreement,testing of all parameters of each product is not necessarily performed.

Reasunos Semiconductor Technology CO.,LTD does not assume any liability arising from the use of any product or circuit designs described herein.Customers are responsible for their products and applications using Reasunos's components.To minimize risk,customers must provide adequate design and operating safeguards.

Reasunos Semiconductor Technology CO.,LTD does not warrant or convey any license eith-er expressed or implied under its patent rights,nor the rights of others.Reproduction of inform-ation in Reasunos's data sheeets or data books is permissible only if reproduction is without modification oralteration.Reproduction of this information with any alteration is an unfair and deceptive business practice. Reasunos Semiconductor Technology CO.,LTD is not responsi-ble or liable for such altered documentation.

Resale of Reasunos's products with statements different from or beyond the parameters stated by Reasunos Semiconductor Technology CO.,LTD for that product or service voids all exp-ress or implied warrantees for the associated Reasunos's product or service and is unfair and deceptive business practice. Reasunos Semiconductor Technology CO.,LTD is not responsi-ble or liable for such statements.

Life Support Policy:

Reasunos Semiconductor Technology CO.,LTD's Products are not authorized for use as cri-tical components in life support devices or systems without the expressed written approval of Reasunos Semiconductor Technology CO.,LTD.

As used herein:

1.Life support devices or systems are devices or systems which:
  a.are intended for surgical implant into the human body,
  b.support or sustain life,
  c.whose failuer to when properly used in accordance with instructions for used provided in the laeling,can be reasonably expected to result in significant injury to the user.

2.A critical component is any component of a life support device or system whose failure to system whose failure to perform can be reasonably expected to cause the failure of the life support device or system,or to affect its safety or effectiveness.