

REASUNOS

RS60N80S

N-Channel Enhancement Mode MOSFET



Lead Free Package and Finish

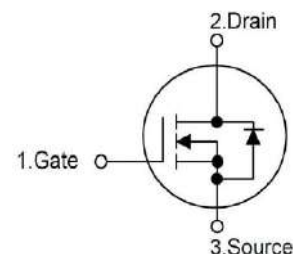
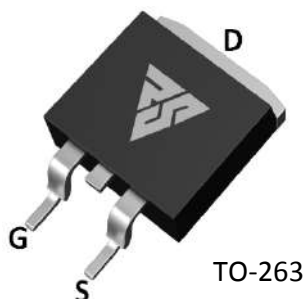
Applications:

- BMSsystem
- LCDMappliances
- High power inverter system

ID	RDS(ON)(Typ.)	VDSS
80A	7mΩ	60V

Features:

- VDS=60V; ID=80A@ VGS=10V
- RDS(ON)<8mΩ @ VGS=10V
- Surface-mounted package
- High UIS and UIS 100% Test
- RoHS Compliant



Not to Scale

Ordering Information

Part Number	Package	Marking
RS60N80S	TO-263	RS60N80S

Absolute Maximun Ratings Tc=25℃ unless otherwise specified

Symbol	Parameter	RS60N80S	Units
VDSS	Drain-to-Source Voltage	60	V
ID	Continuous Drain Current (Tc=25℃)	80	A
	Continuous Drain Current Tc=100℃	60	
IDM	Pulsed Drain Current (Note*1)	320	
PD	Power Dissipation (Tc=25℃)	110	W
VGS	Gate-to-Source Voltage	±20	V
EAS	Single Pulse Avalanche Engergy (Note*2)	390	mJ
TL TPKG	Maximum Temperature for Soldering	300 260	℃
	Leads at 0.063in(1.6mm)from Case for 10 seconds		
	Package Body for 10 seconds		
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

*Drain Current Limited by Maximum Junction Temperature

Caution:Stresses greater than those listed in the“Absolute Maximum Ratings”Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS60N80S	Units	Test Conditions
RθJC	Junction-to-Case	1.36	℃/W	Drain lead soldered to water cooled heatsink,PD adjusted for a peak junction temperature of +150℃.

OFF Characteristics $T_J=25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain-to-source Breakdown Voltage	60	--	--	V	$V_{GS}=0V, I_D=250\mu A$
IDSS	Drain-to-Source Leakage Current	--	--	1	μA	$V_{DS}=60V, V_{GS}=0V$
IGSS	Gate-to-Source Forward Leakage	--	--	100	nA	$V_{GS}=+20V, V_{DS}=0V$
	Gate-to-Source Reverse Leakage	--	--	-100		$V_{GS}=-20V, V_{DS}=0V$

ON Characteristics $T_J=25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain-to-Source On-Resistance	--	7	8	m Ω	$V_{GS}=10V, I_D=20A$
VGS(TH)	Gate Threshold Voltage	2.0	--	4.0	V	$V_{GS}=V_{DS}, I_D=250\mu A$

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn-on Delay Time	--	8.5	--	nS	$V_{DS}=30V$ $I_D=20A$ $V_{GS}=10V$ $R_L=4.5\Omega$ $R_G=1.5\Omega$
trise	Rise Time	--	7	--		
td(OFF)	Turn-OFF Delay Time	--	40	--		
tfall	Fall Time	--	15	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	4000	--	pF	$V_{GS}=0V$ $V_{DS}=30V$ $f=1MHz$
Coss	Output Capacitance	--	290	--		
Crss	Reverse Transfer Capacitance	--	210	--		
Qg	Total Gate Charge	--	90	--	nC	$V_{DS}=30V$ $I_D=20A$ $V_{GS}=10V$
Qgs	Gate-to-Source Charge	--	9	--		
Qgd	Gate-to-Drain("Miller") Charge	--	18	--		

Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
ISD	Source-Drain Current(Body Diode)	--	80	--	A	
ISDM	Pulsed Source-Drain Current(Body Diode)		320	--	A	
VSD	Diode Forward Voltage (Note*3)	--	--	1.2	V	IS=20A,VGS=0V

Notes:

- *1.Repetitive Rating: Pulse width limited by maximum junction temperature
*2.EAS condition: $T_J=25^{\circ}\text{C}$, $L=0.5\text{mH}$, $I_{AS}=30\text{A}$
*3.Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 1.5\%$, $R_G=25\Omega$, Starting $T_J=25^{\circ}\text{C}$

Typical Feature curve

Figure1 Output Characteristics

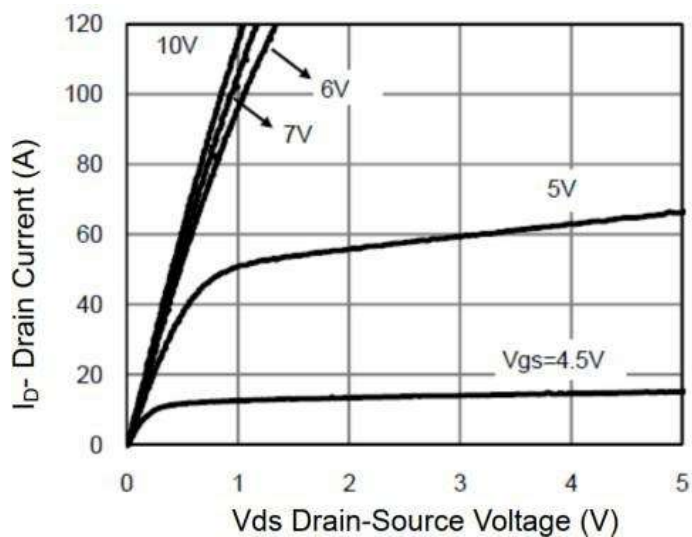


Figure2 Transfer Characteristics

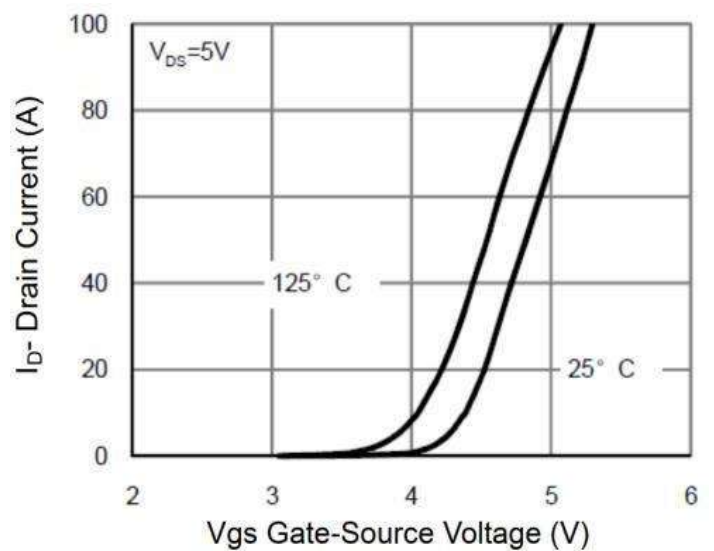


Figure3 On-Resistance vs. I_D and V_{GS}

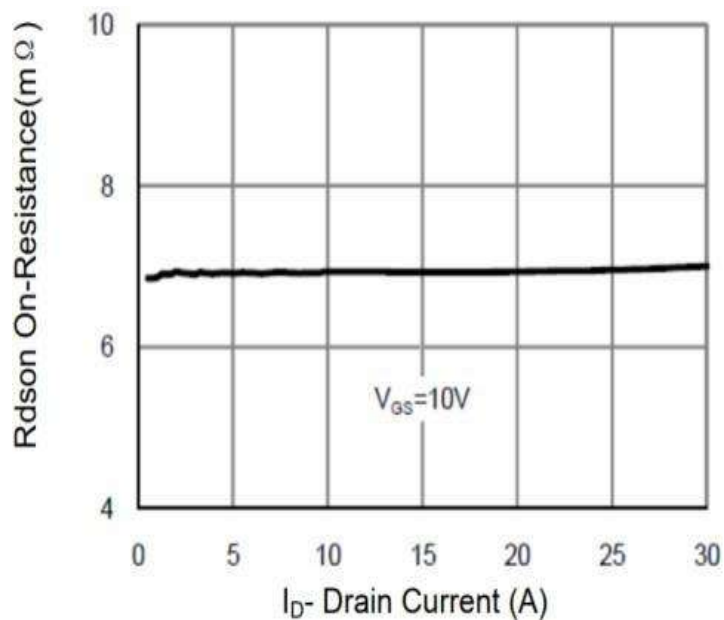


Figure4 On-Resistance vs. Junction Temperature

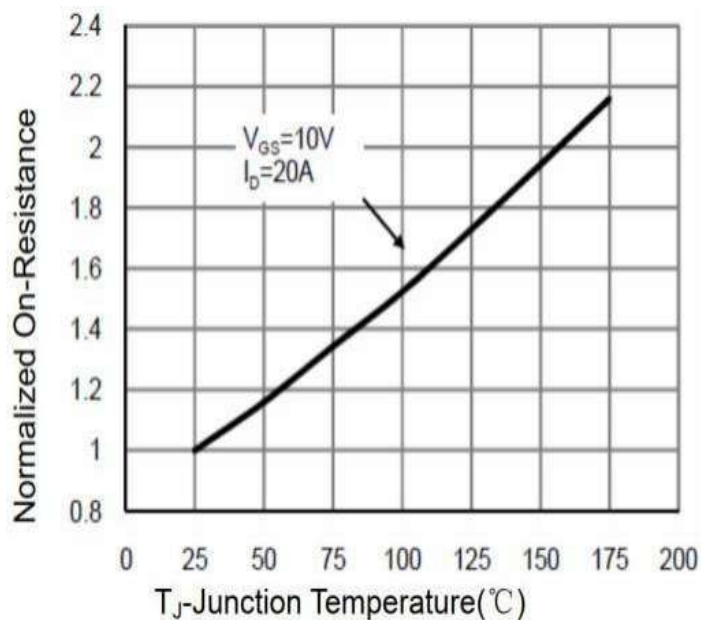


Figure5 On-Resistance vs. V_{GS}

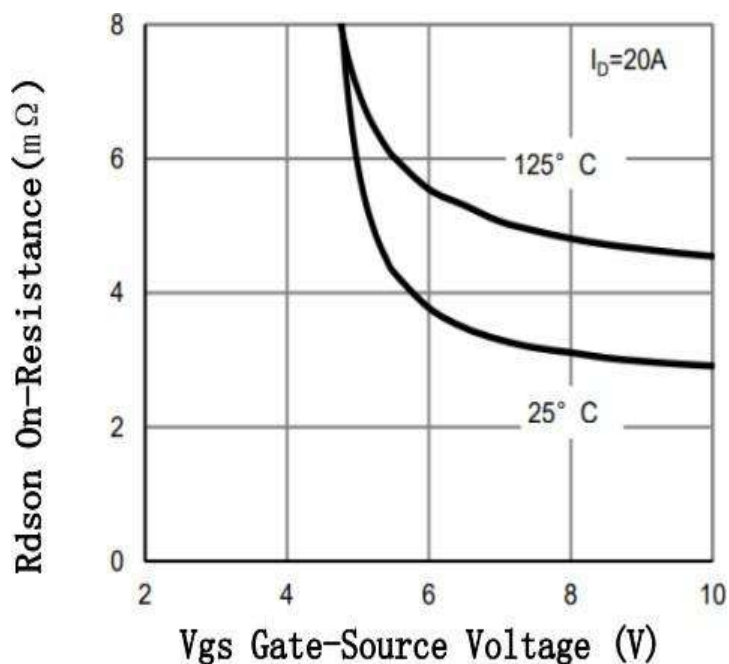


Figure6 Body Diode Forward Voltage

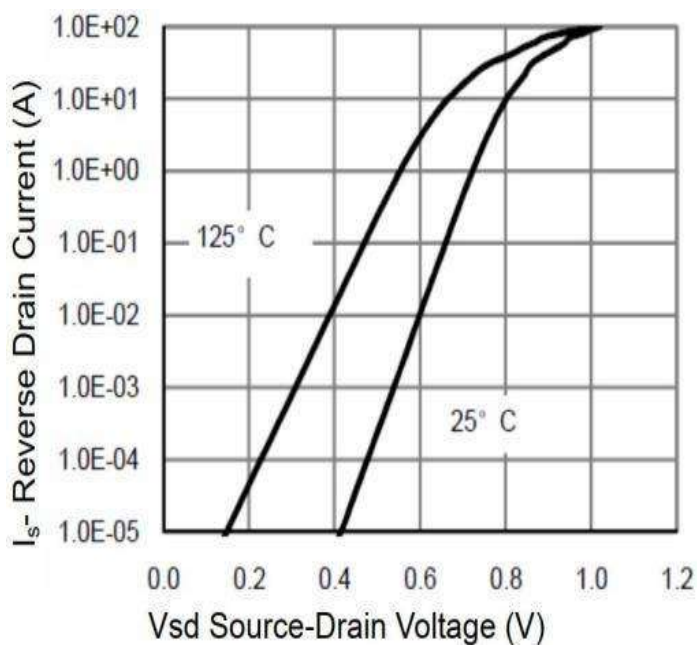


Figure7 Gate-Charge Characteristics

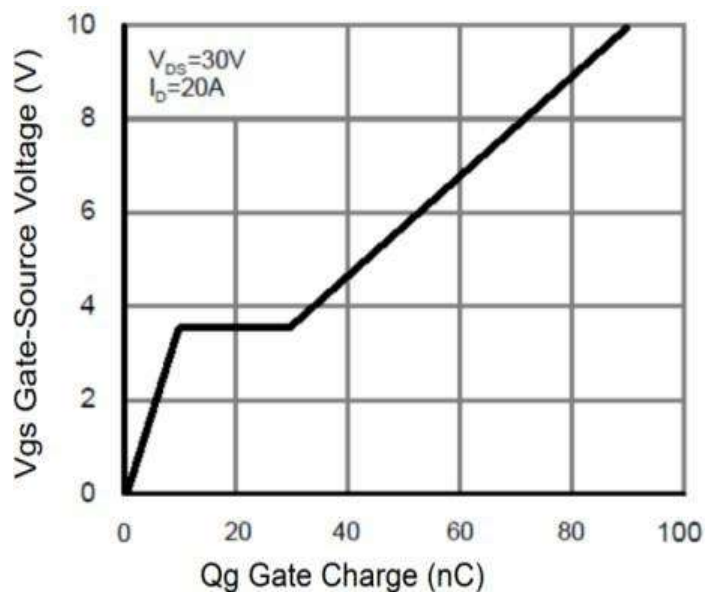


Figure8 Capacitance Characteristics

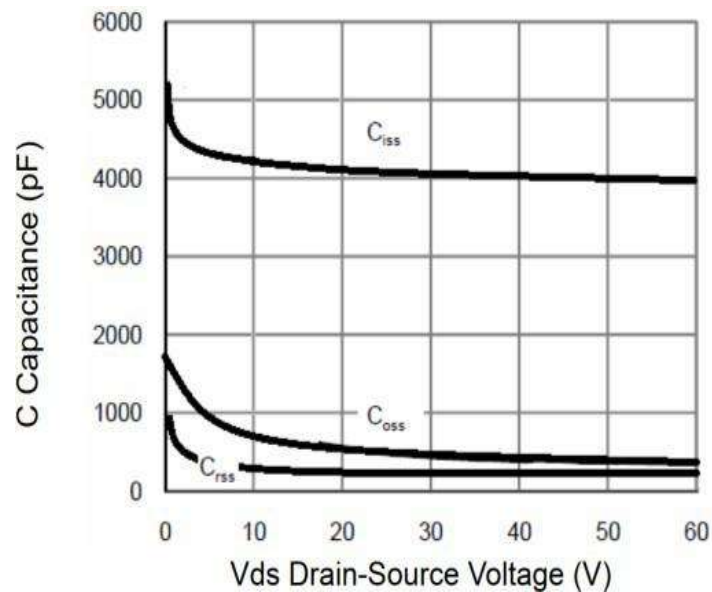


Figure9 Maximum Forward Biased Safe Operation Area

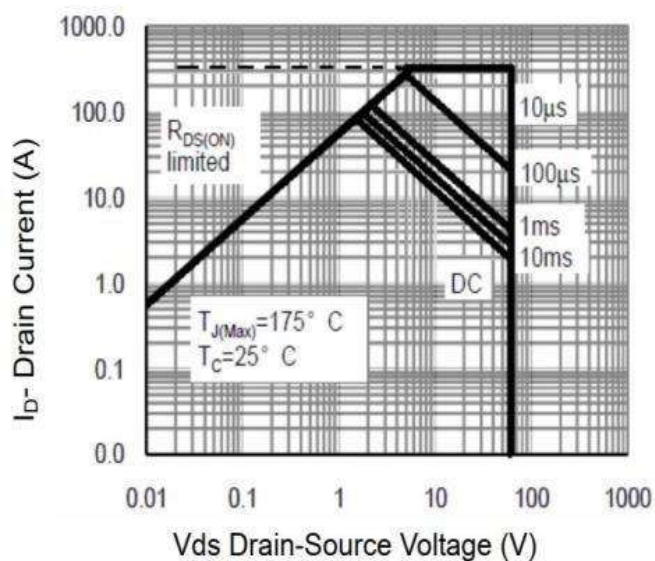
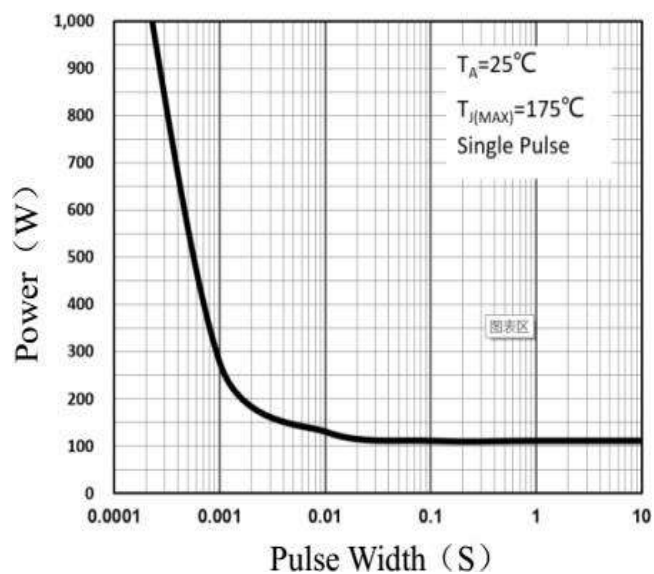


Figure10 Single Pulse Power Rating Junction- to-Ambient



Test Circuits and Waveforms

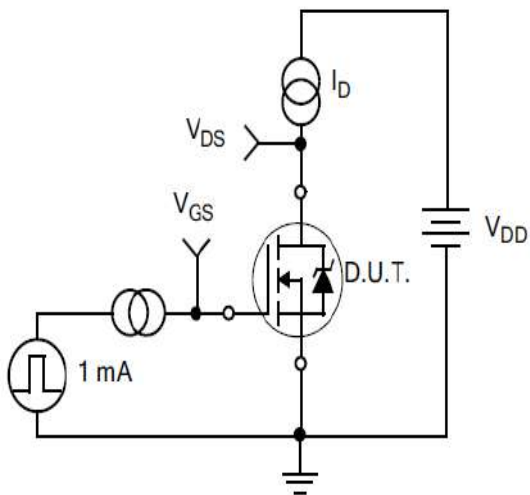


Figure A.
Gate Charge Test Circuit

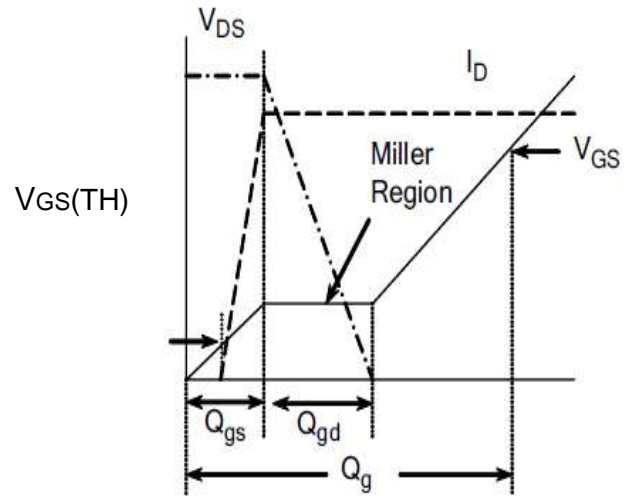


Figure B.
Gate Charge Waveform

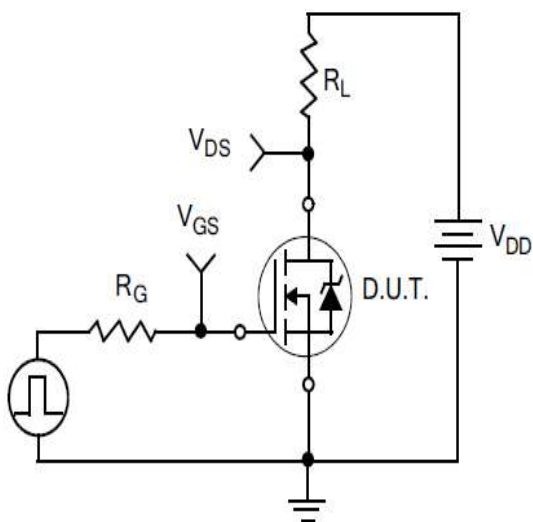


Figure C.
Resistive Switching Test Circuit

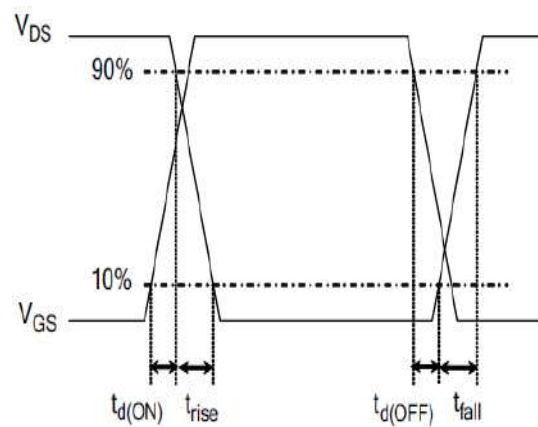


Figure D.
Resistive Switching Waveforms

Test Circuits and Waveforms

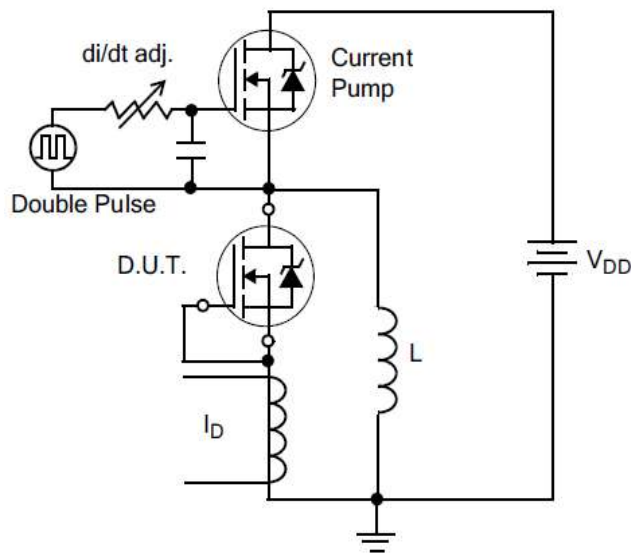


Figure E. Diode Reverse Recovery Test Circuit

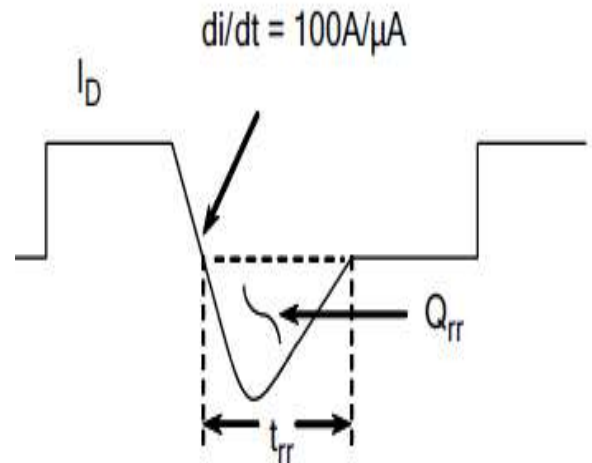


Figure F. Diode Reverse Recovery Waveform

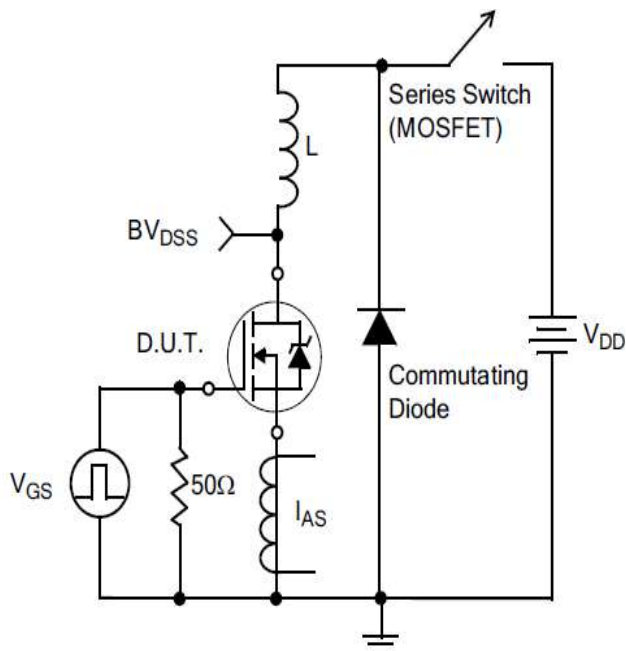
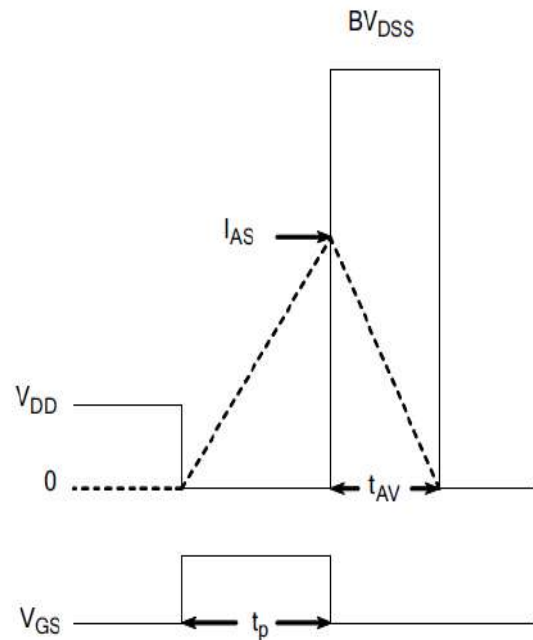


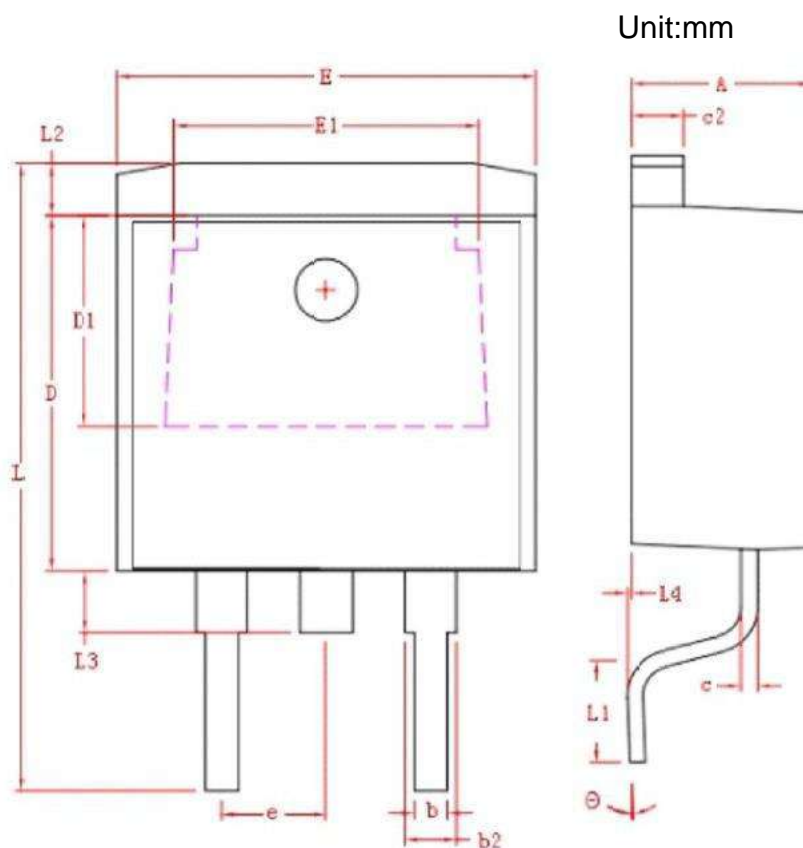
Figure G. Unclamped Inductive Switching Test Circuit



$$E_{AS} = \frac{I_{AS}^2 L}{2}$$

Figure H. Unclamped Inductive Switching Waveforms

Package outline drawing



Symbol	Dimensions In Millimeters	
	MIN.	MAX.
A	4.40	4.80
b	0.76	1.00
L4	0.00	0.25
C	0.36	0.50
L3	1.50 REF	
L1	2.29	2.79
E	9.80	10.40
E1	7.40 REF	
c2	1.25	1.45
b2	1.17	1.47
D	8.60	9.00
D1	5.10 REF	
e	2.54 REF	
L	14.6	15.8
Θ	0° ± 3°	
L2	1.27 REF	

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