REASUNOS

RS60R130F

Multi-Epi Super Junction MOSFET

Lead Free Package and Finish

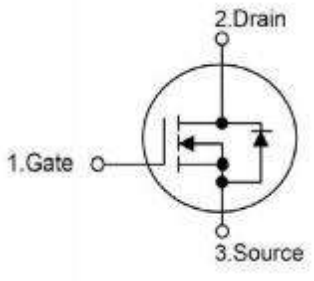
Applications:

- •TV and PC Power
- •Adopter and Lighting
- •Telecom and UPS(Uninterruptible Power Supply)

I_D	$R_{DS(ON)}$(Max.)	V_{DSS}
30A	130mΩ	600V

Features:

- •Low gate charge
- •Better RDS(on) in TO-220F
- •Low RDS(on) per chip area(Low FOM)
- •Very low switching and conduction loss
- •Extremely high commutation ruggedness



Not to Scale

Ordering Information

Part Number	Package	Marking
RS60R130F	TO-220F	RS60R130F

Absolute Maximun Ratings Tc=25℃ unless otherwise specified

Symbol	Parameter	RS60R130F	Units
VDSS	Drain-to-Source Voltage	600	V
ID	Continuous Drain Current (TC = 25℃)	30	A
	Continuous Drain Current (TC = 100℃)	19.5	
IDM	Pulsed Drain Current (Note*1)	90	
PD	Power Dissipation(Tc=25℃)	34	W
VGS	Gate-to-Source Voltage	±30	V
EAS	Single Pulse Avalanche Engergy (Note*2)	330	mJ
TL TPKG	Maximum Temperature for Soldering Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	300 260	℃
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

*Drain Current Limited by Maximum Junction Temperature

Caution:Stresses greater than those listed in the"Absolute Maximum Ratings"Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS60R130F	Units	Test Conditions
RθJC	Junction-to-Case	3.7	℃/W	Drain lead soldered to water cooled heatsink,PD Adjusted for a peak junction temperature of +150℃.
RθJA	Junction-to-Ambient	80		1 cubic foot chamber,free air.

OFF Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain-to-source Breakdown Voltage	600	--	--	V	VGS = 0V, ID = 250μA, TJ= 25℃
		--	600	--	V	VGS = 0V, ID = 250μA, TJ= 150℃
IDSS	Drain-to-Source Leakage Current	--	--	1.0	μA	VDS=600V,VGS=0V
IGSS	Gate-to-Source Forward Leakage	--	--	100	nA	VGS=+30V ,VDS=0V
	Gate-to-Source Reverse Leakage	--	--	-100		VGS=-30V ,VDS=0V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain-to-Source On-Resistance	--	120	130	mΩ	VGS=10V,ID=15A
VGS(TH)	Gate Threshold Voltage	2.0	--	4.0	V	VGS=VDS,ID=250μA
R_G	Gate Resistance	--	4.5	--	Ω	VGS= 0V,f = 1.0MHz

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn-on Delay Time	--	30	--	ns	VDS=300V ID=30A RG=25Ω VGS=10V
trise	Rise Time	--	45	--		
td(OFF)	Turn-OFF Delay Time	--	145			
tfall	Fall Time	--	36			

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	1910	--	pF	VGS=0V VDS=50V f=1.0MHz
Coss	Output Capacitance	--	125	--		
Crss	Reverse Transfer Capacitance	--	3	--		
Qg	Total Gate Charge	--	50	--	nC	VDS=480V ID=30A VGS=10V
Qgs	Gate-to-Source Charge	--	10	--		
Qgd	Gate-to-Drain("Miller"）Charge	--	14	--		

Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current	--	--	30	A	Integral pn-diode in MOSFET
ISM	Maximum Pulsed Current	--	--	90	A	
VSD	Diode Forward Voltage	--	--	1.4	V	IS=30A,VGS=0V Tj=25℃
trr	Reverse Recovery Time	--	445	--	nS	VR=100V,VGS=0V IS=30A,di/dt=100A/μs
Qrr	Reverse Recovery Charge	--	6.4	--	μC	
Irrm	Peak Reverse Recovery Current	--	35	--	A	

Notes:

*1.Repetitive rating;pulse width limited by maximum junction temperature.

*2.Tj=25?C, IAS=2.0A, VDD=50V,ID=IAR.

Typical Feature curve T_J=25℃, unless otherwise noted

Figure1. Output Characteristics

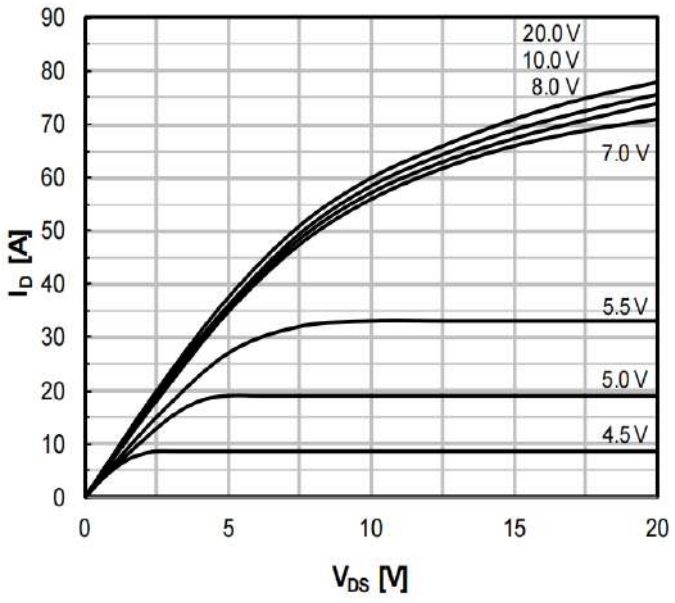


Figure2. Transfer Characteristics

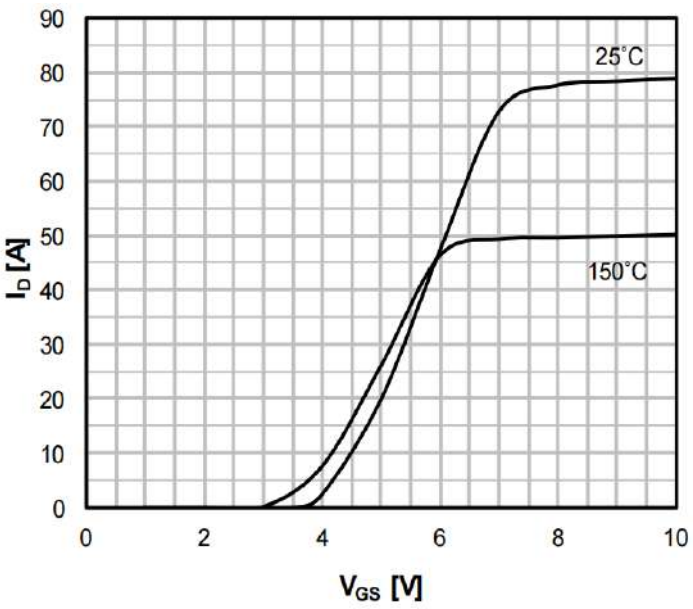


Figure 3. On-Resistance VS.Drain Current

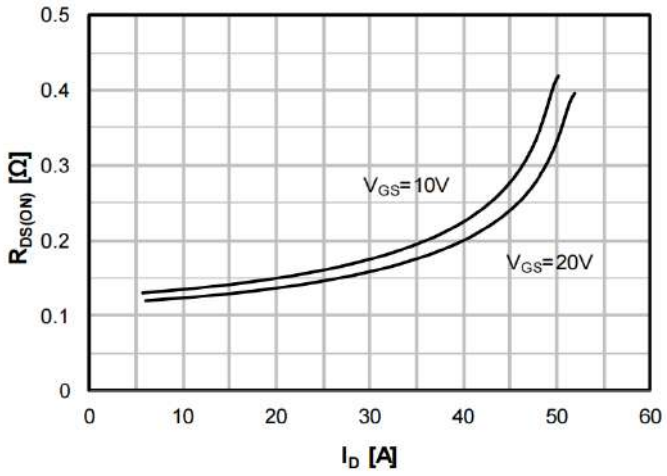


Figure 4. Capacitance

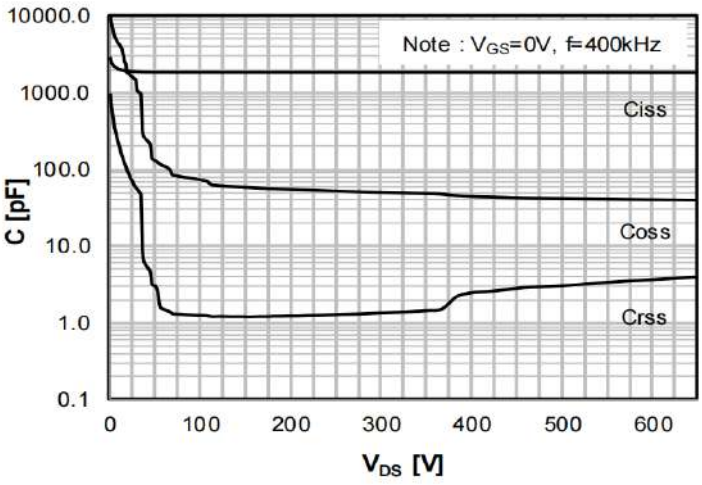


Figure 5. Gate Charge

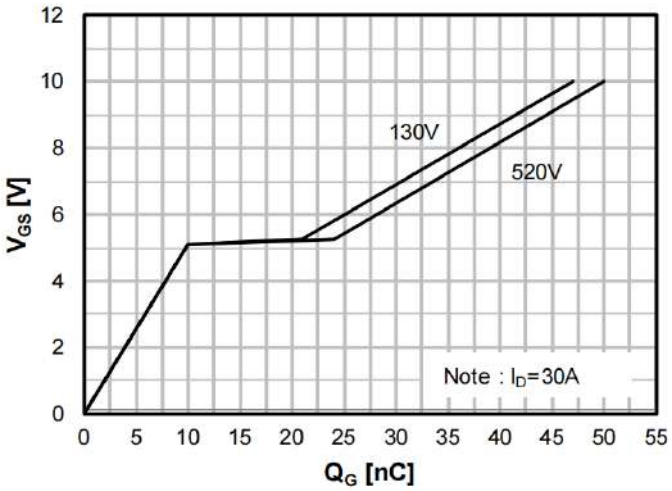


Figure 6.Body Diode Forward Voltage

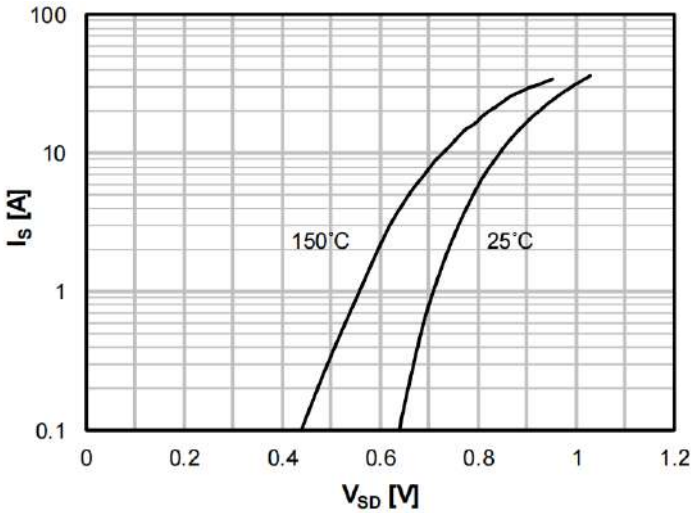


Figure 7.On-Resistan ce vs. Junction Temperature

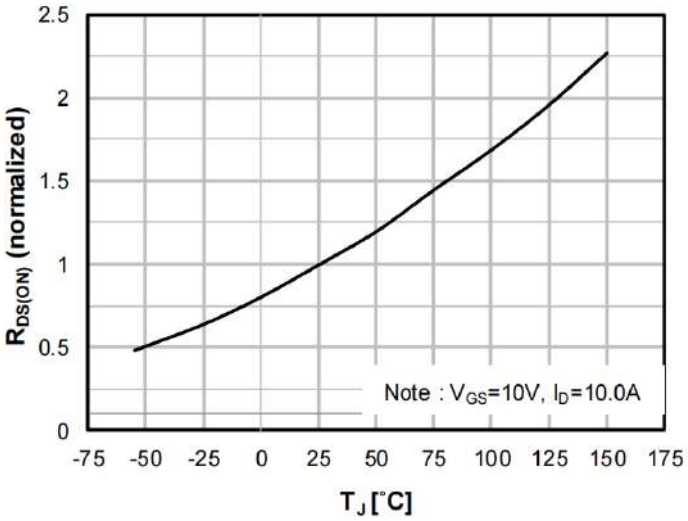


Figure 8.Bearkdown Voltage vs. Junction Temperature

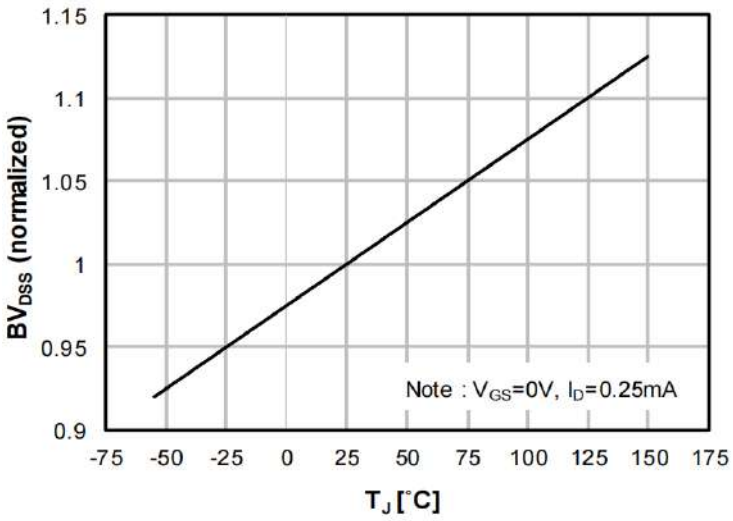


Figure 9.Safe operation area

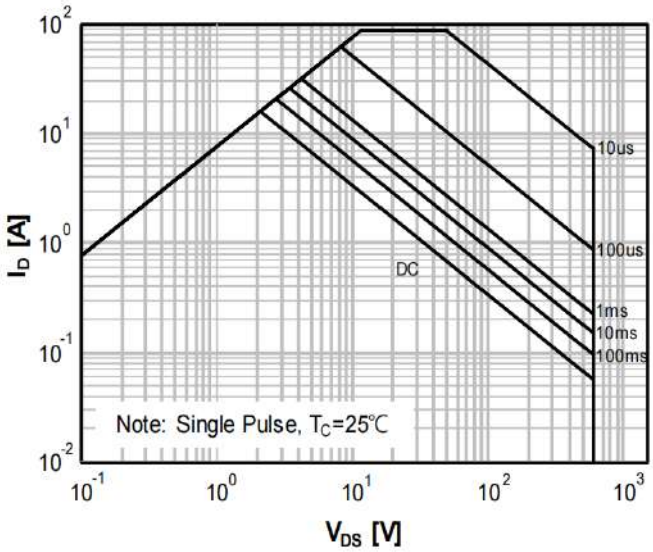
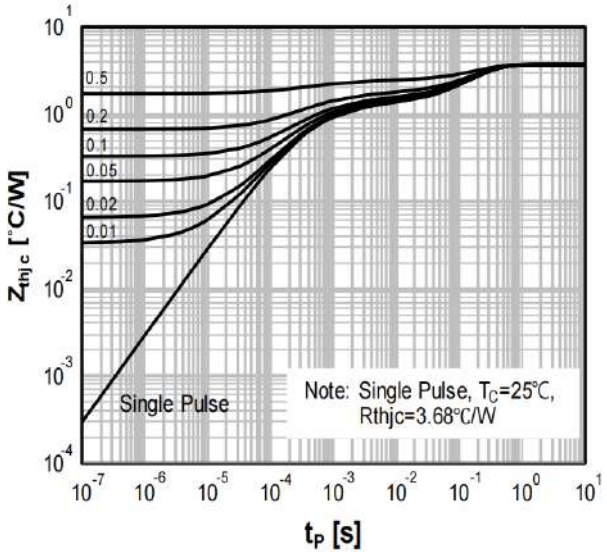


Figure 10.Transient Thermal Impedance



Test Circuits and Waveforms

Figure A: Gate Charge Test Circuit and Waveform

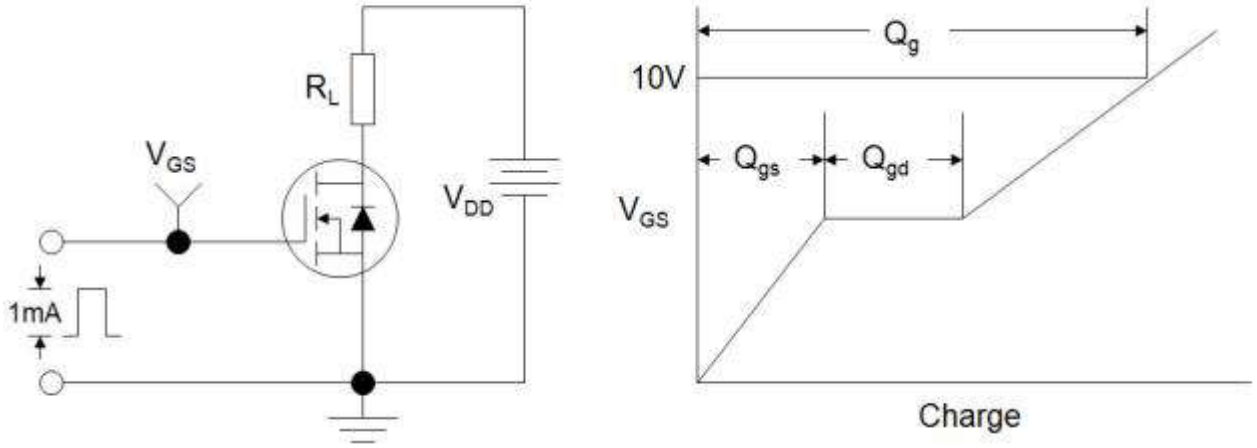


Figure B: Resistive Switching Test Circuit and Waveform

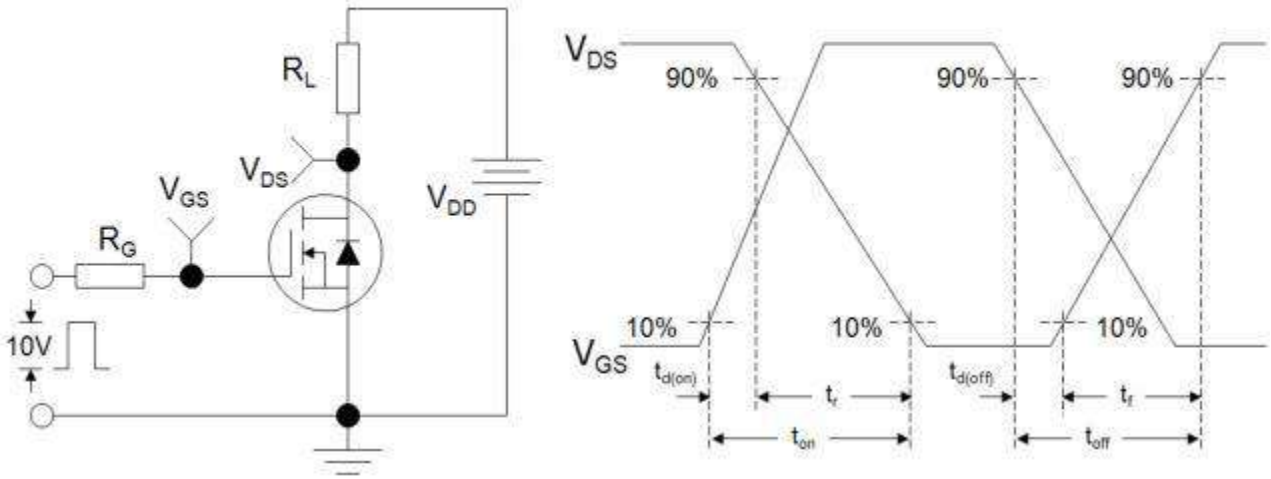
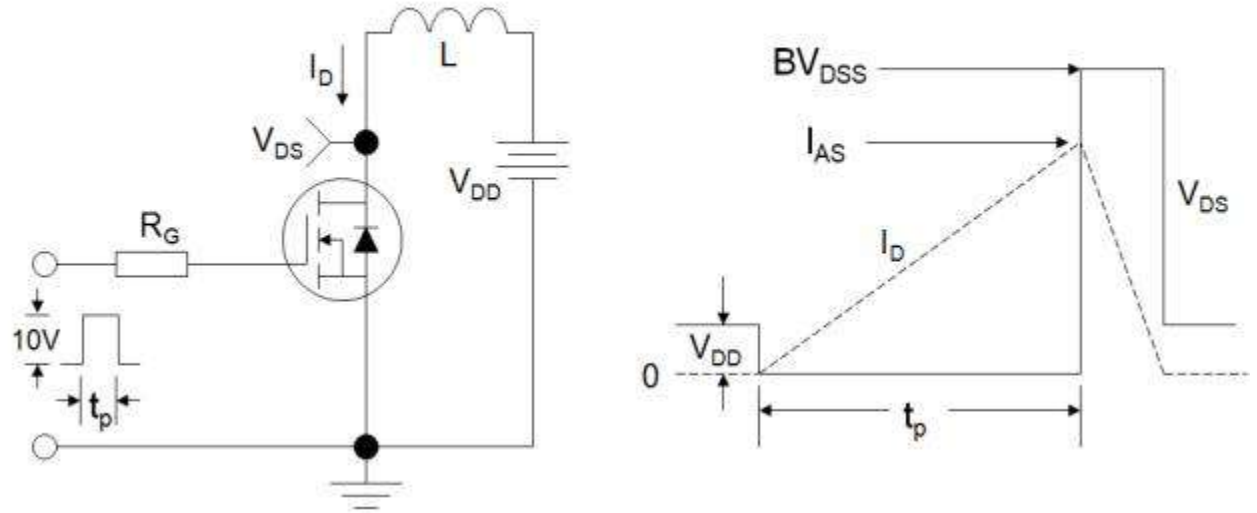
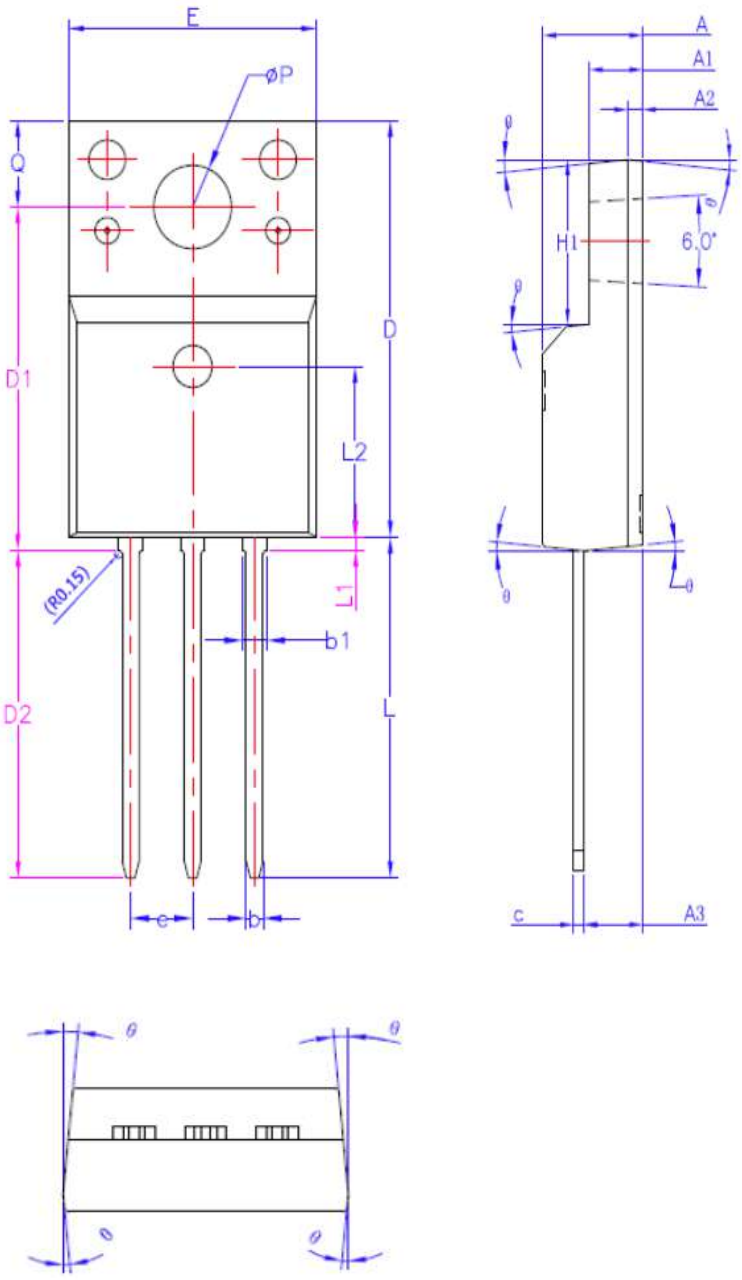


Figure C: Unclamped Inductive Switching Test Circuit and Waveform



Package outline drawing

Unit:mm



项目	规范(mm)	
	MIN	MAX
A	4.50	4.83
A1	2.34	2.74
A2	0.70 REF	
A3	2.56	2.93
b	0.60	0.80
b1	0.90	1.10
c	0.45	0.60
D	15.67	16.07
D1	12.87	13.27
D2	12.28	12.68
E	9.96	10.36
e	2.54 BSC	
H1	6.48	6.88
L	12.68	13.28
L1	-	0.85
L2	6.50 REF	
ϕP	3.08	3.28
Q	3.20	3.40
θ 1	1°	5°

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