REASUNOS

RS65R099W

Multi-Epi Super Junction MOSFET

Lead Free Package and Finish

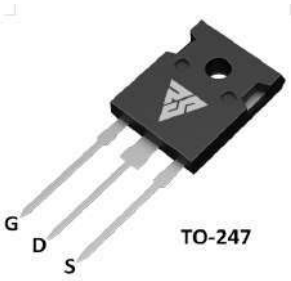
Applications:

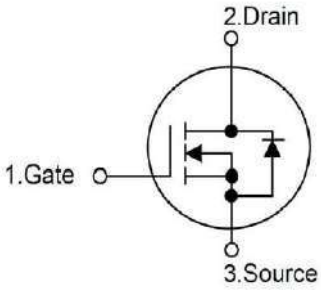
- •PFC Power Supply Stages
- •Switching Applications
- •Adapter
- •LED Lighting Power

I_D	$R_{DS(ON)}$(Typ.)	V_{DSS}
40A	86mΩ	650V

Features:

- •Low Power Loss by High Speed Switching
- •Low On-Resistance
- •100% Avalanche Tested
- •RoHS Compliant





Not to Scale

Ordering Information:

Part Number	Package	Marking
RS65R099W	TO-247	RS65R099W

Absolute Maximun Ratings Tc=25℃ unless otherwise specified

Symbol	Parameter	RS65R099W	Units
V_{DSS}	Drain-to-Source Voltage	650	V
I_D	Continuous Drain Current	40	A
I_D@ 100 ℃	Continuous Drain Current	26	
I_{DM}	Pulsed Drain Current (Note*1)	120	
P_D	Power Dissipation	278	W
V_{GS}	Gate-to-Source Voltage	±30	V
E_{AS}	Single Pulse Avalanche Engergy (Note*2)	1000	mJ
T_L T_{PKG}	Maximum Temperature for Soldering Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	300 260	℃
T_J and T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	

*Drain Current Limited by Maximum Junction Temperature

Caution:Stresses greater than those listed in the“Absolute Maximum Ratings”Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS65R099W	Units	Test Conditions
RθJC	Junction-to-Case	0.45	℃/W	Drain lead soldered to water cooled heatsink,PD adjusted for a peak junction temperature of +150℃.
RθJA	Junction-to-Ambient	62		1 cubic foot chamber,free air.

OFF Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-source Breakdown Voltage	650	--	--	V	V_{GS}=0V,I_D=250μA
I_{DSS}	Drain-to-Source Leakage Current	--	--	10	μA	V_{DS}=650V,V_{GS}=0V
I_{GSS}	Gate-to-Source Forward Leakage	--	--	100	μA	V_{GS}=+30V V_{DS}=0V
	Gate-to-Source Reverse Leakage	--	--	-100		V_{GS}=-30V V_{DS}=0V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	--	0.086	0.099	Ω	V_{GS}=10V,I_D=20A
$V_{GS(TH)}$	Gate Threshold Voltage	2.5	--	5.0	V	V_{GS}=V_{DS},I_D=250μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	31	--	nS	V_{DS}=400V I_D=20A R_G=10Ω VGS= 10V
t_{rise}	Rise Time	--	44	--		
$t_{d(OFF)}$	Turn-OFF Delay Time	--	151	--		
t_{fall}	Fall Time	--	12.3	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
C_{iss}	Input Capacitance	--	3270	--	pF	V_{GS}=0V V_{DS}=100V f=250KHz
C_{oss}	Output Capacitance	--	116	--		
C_{rss}	Reverse Transfer Capacitance	--	3.2	--		
Q_g	Total Gate Charge	--	66	--	nC	V_{DS}=400V I_D=20A V_{GS}=10V
Q_{gs}	Gate-to-Source Charge	--	18	--		
Q_{gd}	Gate-to-Drain("Miller"）Charge	--	25	--		

Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current	--	--	40	A	Integral pn-diode in MOSFET
I_{SM}	Maximum Pulsed Current	--	--	140	A	
V_{SD}	Diode Forward Voltage	--	--	1.2	V	IS=20A,VGS=0V
t_{rr}	Reverse Recovery Time	--	198	--	nS	VGS=0V IS=20A,di/dt=100A/μs
Q_{rr}	Reverse Recovery Charge	--	1.48	--	μC	

Notes:

*1. Repetitive rating;pulse width limited by maximum junction temperature.
*2. IAS=8A,VDD=60V,RG=25Ω,StartingTJ=25°C.

Typical Feature curve

Figure 1. On-Region Characteristics

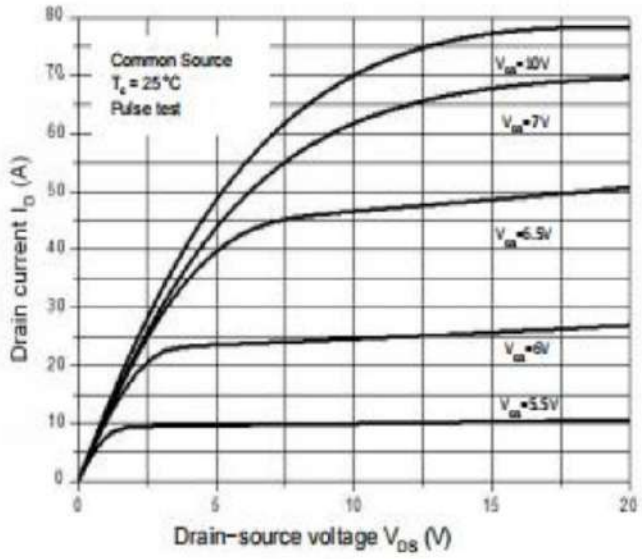


Figure 2. Transfer Characteristics

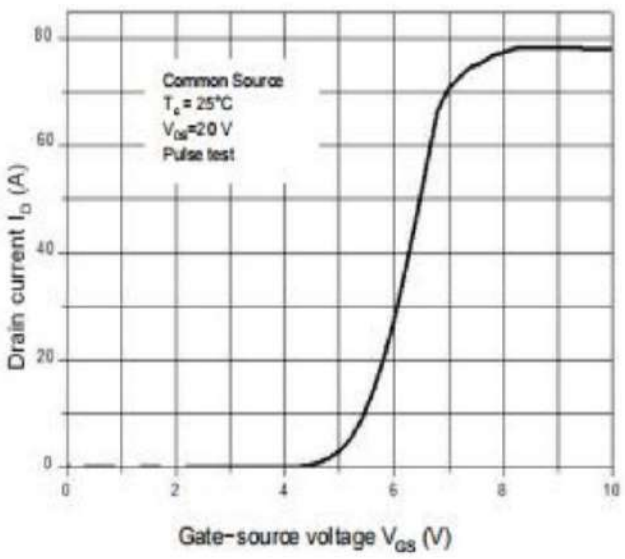


Figure 3. On-Resistance Variation vs. Drain Current

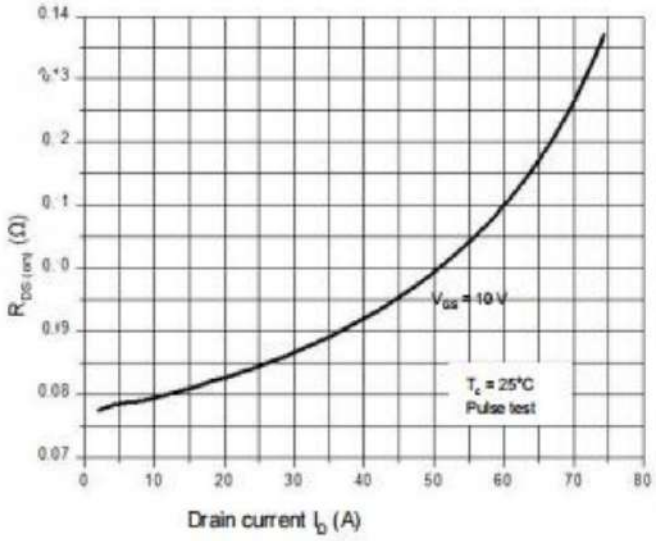


Figure 4. Threshold Voltage vs. Temperature

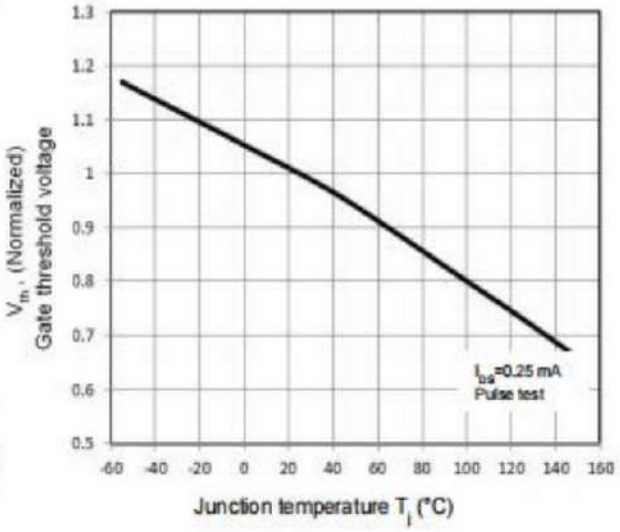


Figure 5. Breakdown Voltage vs. Temperature

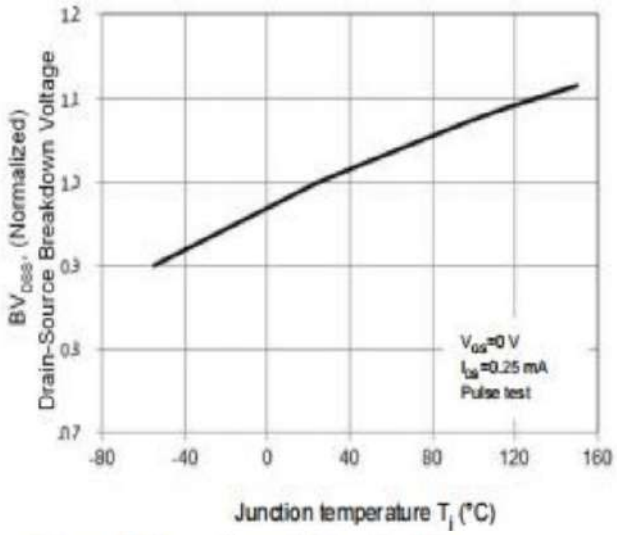


Figure 6. On-Resistance vs. Temperature

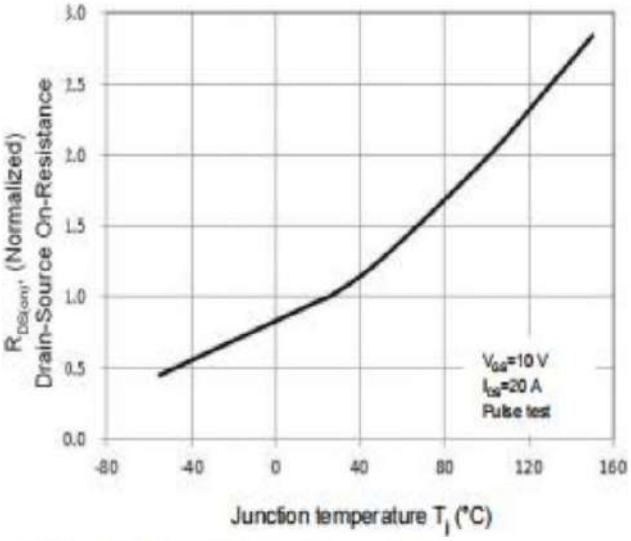


Figure 7. Capacitance Characteristics

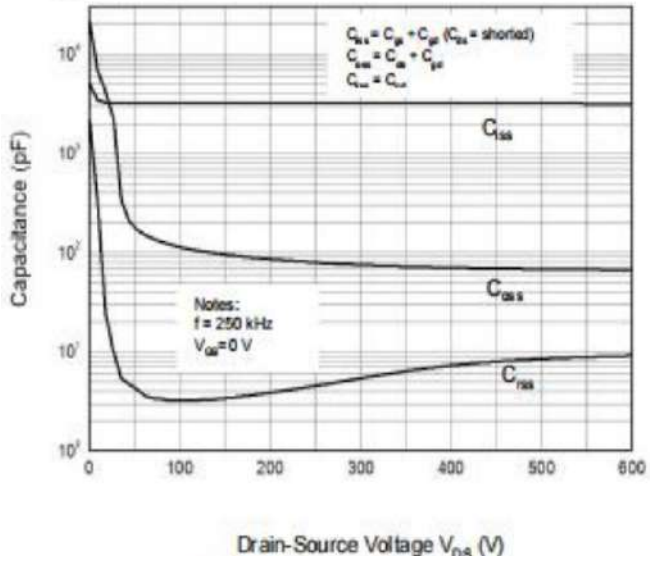


Figure 8. Gate Charge Characterist

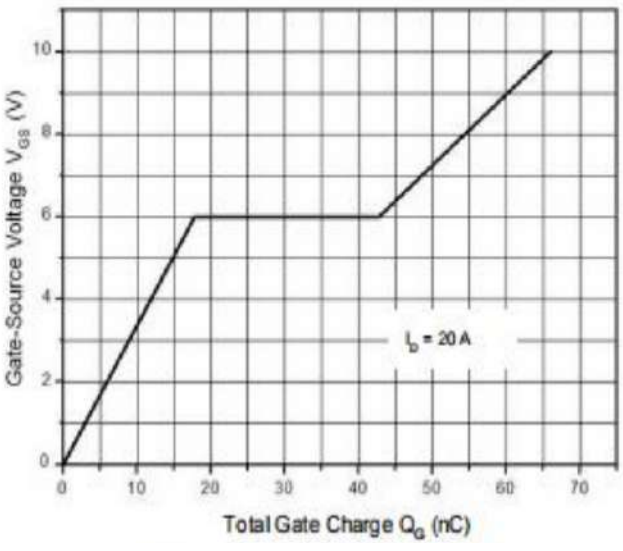


Figure 9. Maximum Safe Operating Area

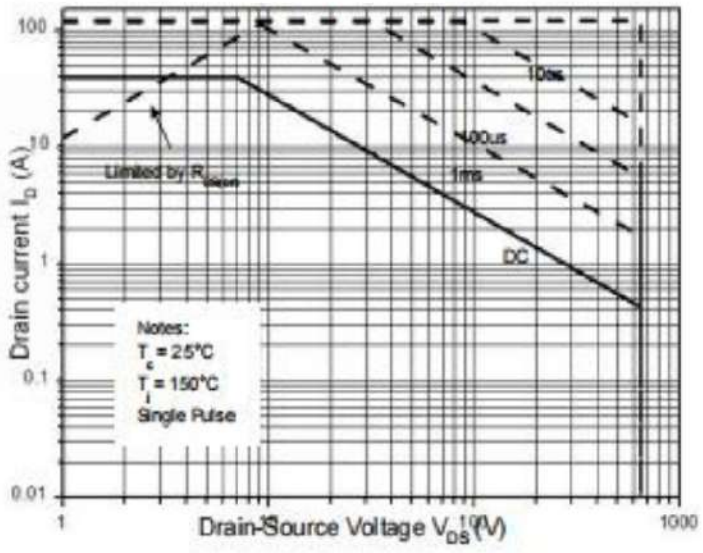
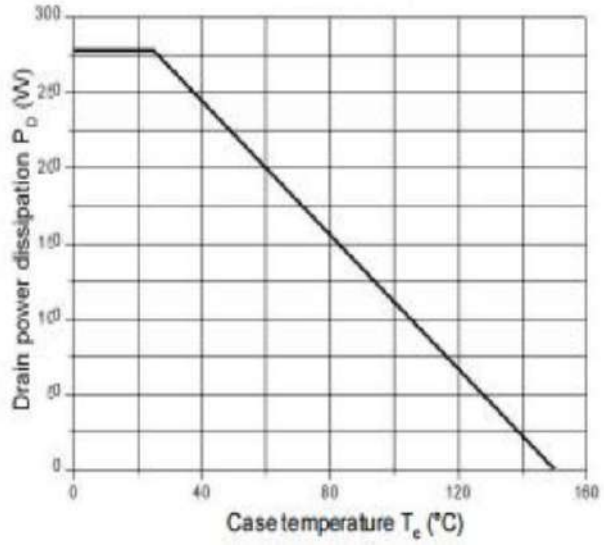


Figure 10.Power Dissipation vs. Temperature



Test Circuits and Waveforms

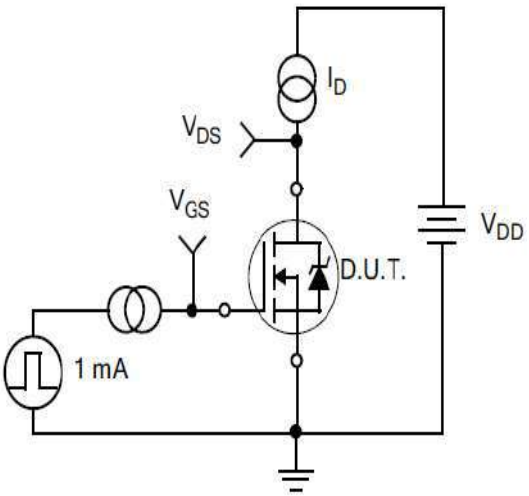


Figure A.
Gate Charge Test Circuit

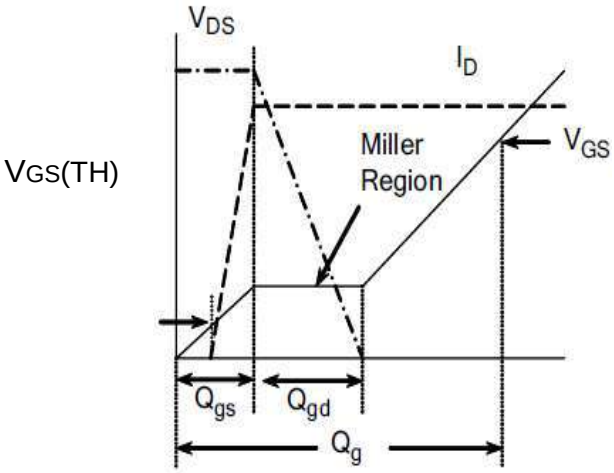


Figure B.
Gate Charge Waveform

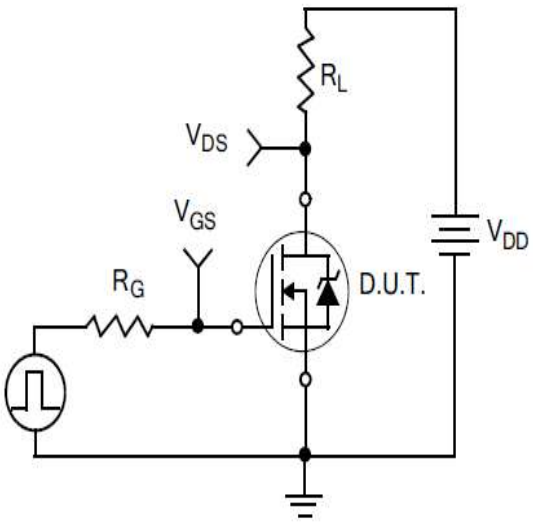


Figure C.
Resistive Switching Test Circuit

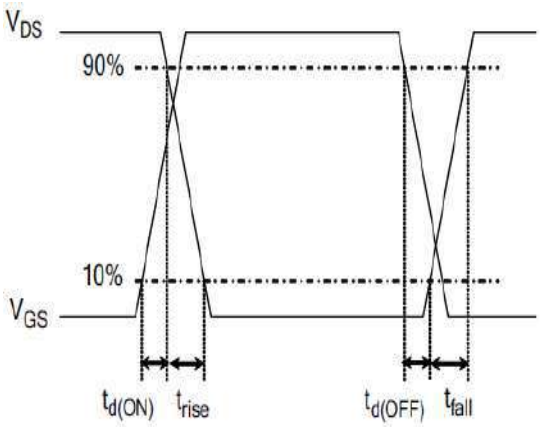


Figure D.
Resistive Switching Waveforms

Test Circuits and Waveforms

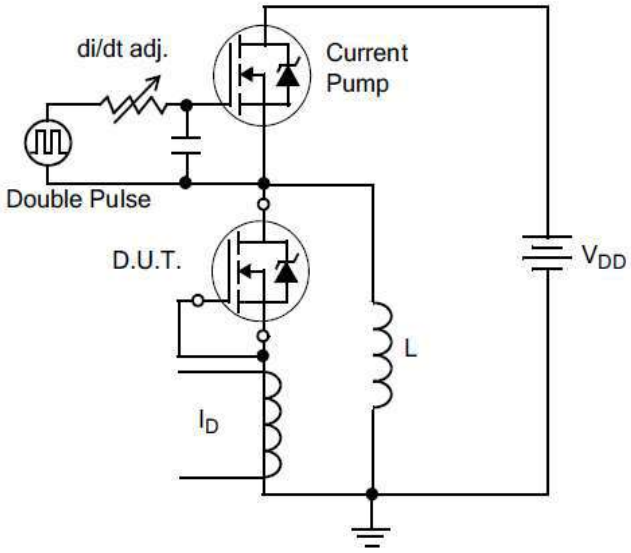


Figure E.Diode Reverse Recovery Test Circuit

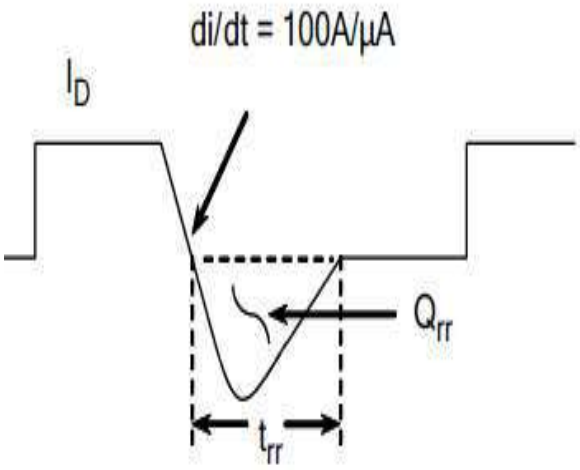


Figure F.Diode Reverse Recovery Waveform

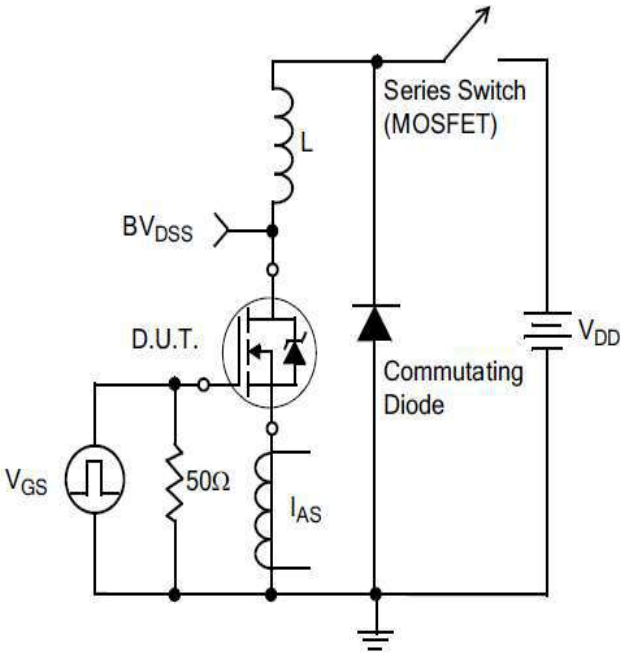
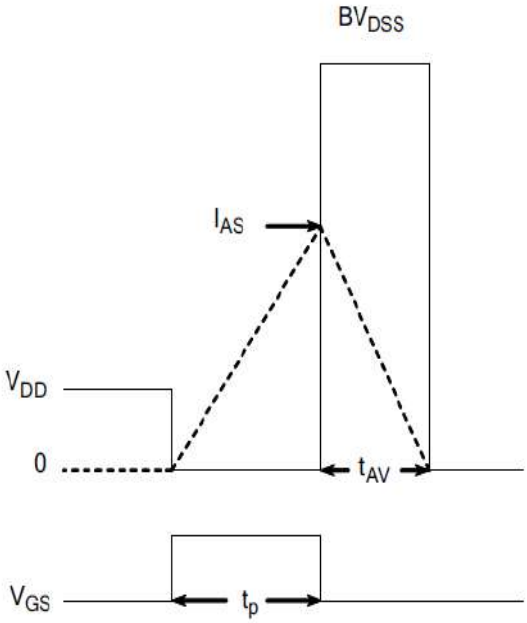


Figure G.Unclamped Inductive Switching Test Circuit

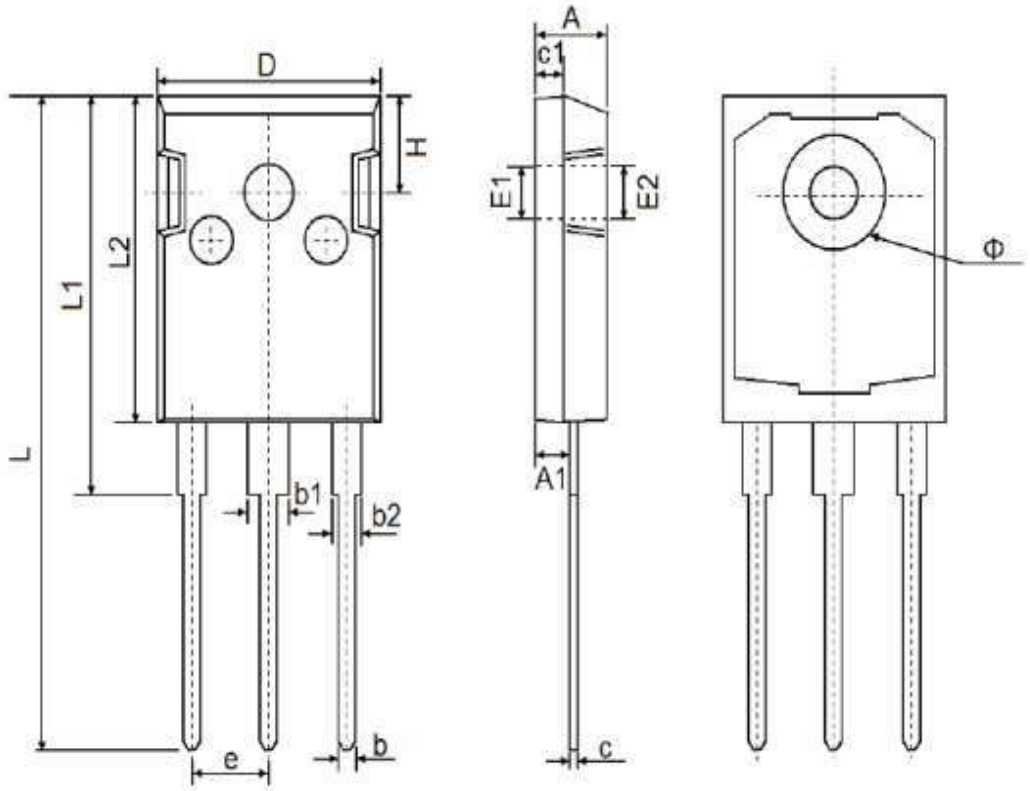


$$E_{AS}=\frac{I_{AS}^2 L}{2}$$

Figure H.Unclamped Inductive Switching Waveforms

Package outline drawing

Unit:mm



TO-247

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.850	5.150	0.191	0.200
A1	2.200	2.600	0.087	0.102
b	1.000	1.400	0.039	0.055
b1	2.800	3.200	0.110	0.126
b2	1.800	2.200	0.071	0.087
c	0.500	0.700	0.020	0.028
c1	1.900	2.100	0.075	0.083
D	15.450	15.750	0.608	0.620
E1	3.500 REF		0.138 REF	
E2	3.600 REF		0.142 REF	
L	40.900	41.300	1.610	1.626
L1	24.800	25.100	0.976	0.988
L2	20.300	20.600	0.799	0.811
Φ	7.100	7.300	0.280	0.287
e	5.450 TYP		0.215 TYP	
H	5.980 REF		0.235 REF	

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