REASUNOS

RS6N70D

700V N Channel MOSFET

Lead Free Package and Finish

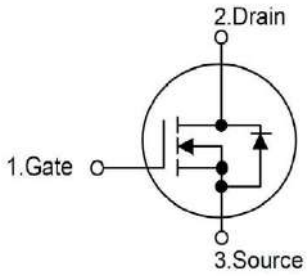
Applications:

•Switch Mode Power Supply(SMPS)
•Uninterruptible Power Supply(UPS)
•Power Factor Correction(PFC)

I_D	$R_{DS(ON)}$(Typ.)	V_{DSS}
6A	1.3Ω	700V

Features:

•improved dv/dt capability
•100% avalanche tested
•Fast switching
•RoHS Compliant



Not to Scale

Ordering Information

Part Number	Package	Marking
RS6N70D	TO-252	RS6N70D

Absolute Maximun Ratings Tc=25℃ unless otherwise specified

Symbol	Parameter	RS6N70D	Units
V_{DSS}	Drain-to-Source Voltage (Note*1)	700	V
I_D	Continuous Drain Current	6	A
I_{DM}	Pulsed Drain Current (Note*2)	24	
PD	Power Dissipation(Tc=25℃)	63	W
VGS	Gate-to-Source Voltage	±30	V
EAS	Single Pulse Avalanche Engergy IAS=6A VDD=50V RG=25Ω TJ=25℃	198	mJ
IAR	Avalanche Current	4.5	A
EAR	Repetitive Avalanche Engergy	40	mJ
TL TPKG	Maximum Temperature for Soldering Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	300 260	℃
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

*Drain Current Limited by Maximum Junction Temperature

Caution:Stresses greater than those listed in the“Absolute Maximum Ratings”Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS6N70D	Units	Test Conditions
$R_{\theta JC}$	Junction-to-Case	1.29	℃/W	Drain lead soldered to water cooled heatsink,PD Adjusted for a peak junction temperature of +150℃.
$R_{\theta JA}$	Junction-to-Ambient	60		1 cubic foot chamber,free air.

OFF Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-source Breakdown Voltage	700	--	--	V	V_{GS}=0V,I_D=250μA
I_{DSS}	Drain-to-Source Leakage Current	--	--	1.0	μA	V_{DS}=700V,V_{GS}=0V
I_{GSS}	Gate-to-Source Forward Leakage	--	--	100	nA	V_{GS}=+30V V_{DS}=0V
	Gate-to-Source Reverse Leakage	--	--	-100		V_{GS}=-30V V_{DS}=0V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	--	1.3	1.6	Ω	V_{GS}=10V,I_D=3.0A
$V_{GS(TH)}$	Gate Threshold Voltage	2.0	--	4.0	V	V_{GS}=V_{DS},I_D=250μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	18	--	ns	V_{DS}=350V I_D=6A R_G=25Ω
t_{rise}	Rise Time	--	26	--		
$t_{d(OFF)}$	Turn-OFF Delay Time	--	86	--		
t_{fall}	Fall Time	--	36	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
C_{iss}	Input Capacitance	--	1041	--	pF	V_{GS}=0V V_{DS}=25V f=1.0MHz
C_{oss}	Output Capacitance	--	92.7	--		
C_{rss}	Reverse Transfer Capacitance	--	5.9	--		
Q_g	Total Gate Charge	--	24.2	--	nC	V_{DS}=560V I_D=6A V_{GS}=10V
Q_{gs}	Gate-to-Source Charge	--	5.0	--		
Q_{gd}	Gate-to-Drain("Miller"）Charge	--	10.9	--		

Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current	--	--	6	A	Integral pn-diode in MOSFET
I_{SM}	Maximum Pulsed Current	--	--	24	A	
V_{SD}	Diode Forward Voltage	--	--	1.4	V	I_S=6A,V_{GS}=0V Tj=25℃
t_{rr}	Reverse Recovery Time	--	310	--	nS	V_{GS}=0V I_S=6A,di/dt=100A/μs
Q_{rr}	Reverse Recovery Charge	--	4.3	--	μC	

Notes:

*1.TJ=±25℃ to +150℃.
*2.Repetitive rating;pulse width limited by maximum junction temperature.
*3.Pulse width≤300μs;duty cycle ≤1%.

Typical Feature curve T_J=25℃, unless otherwise noted

Figure1.Typical Output Characteistics

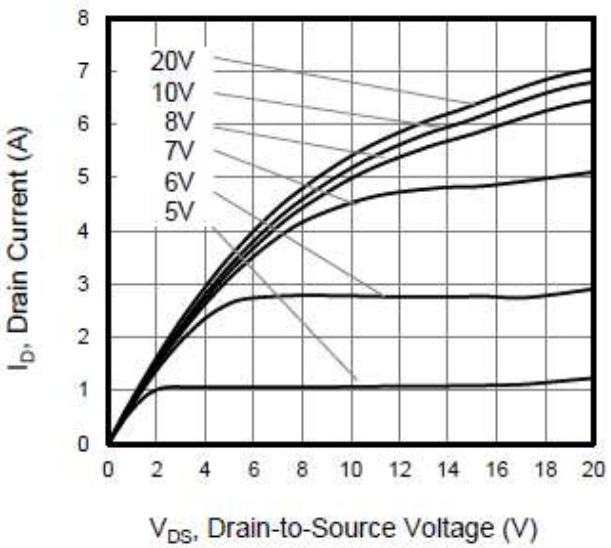
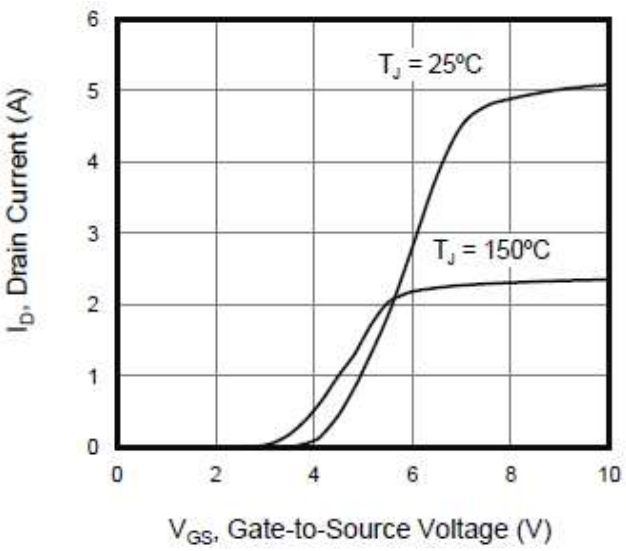
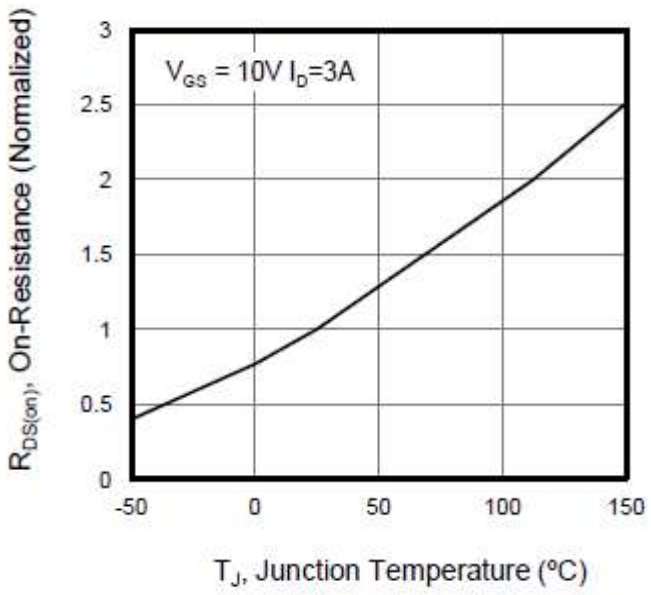


Figure2.Typical Transfer Characteristics



Figuer3.Typical ON-Resistance vs Temperature



Figuer4.Typical Body Diode Forward Voltage

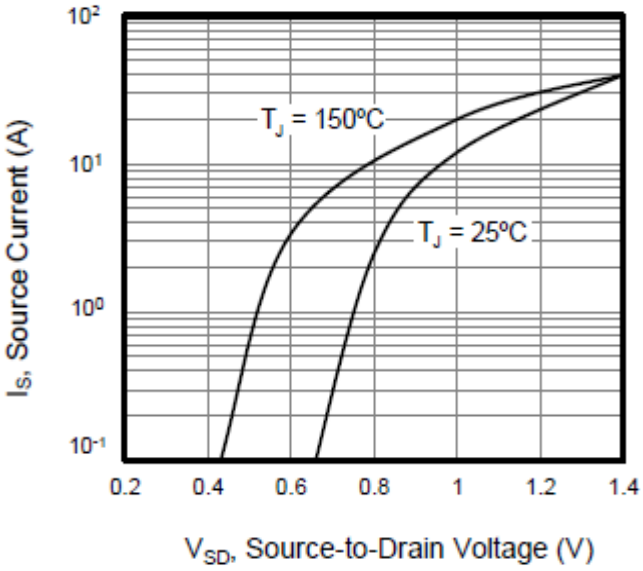


Figure5.Typical Temperature vs Drain Current

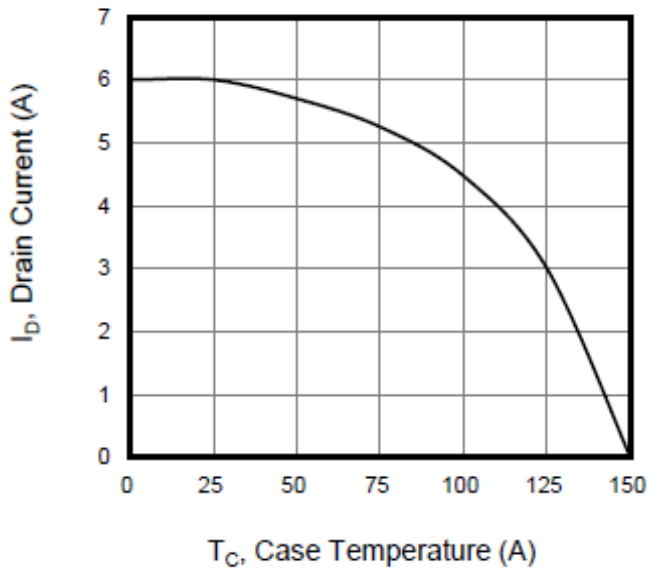


Figure6.Typical Temperature vs BVdss Variation

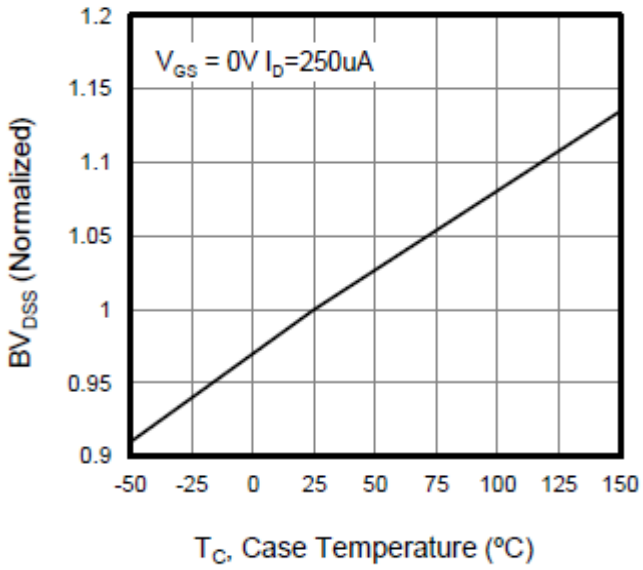


Figure7. Typical Capacitance vs Drain-to-Source Voltage

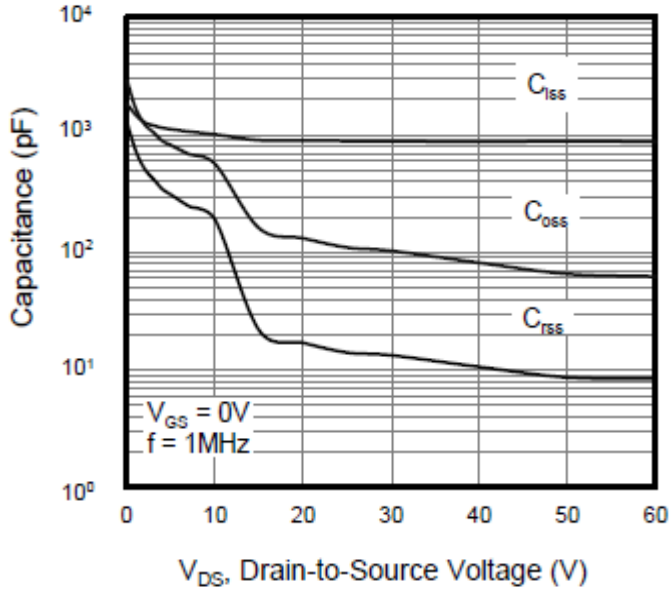


Figure8. Typical Gate Charge

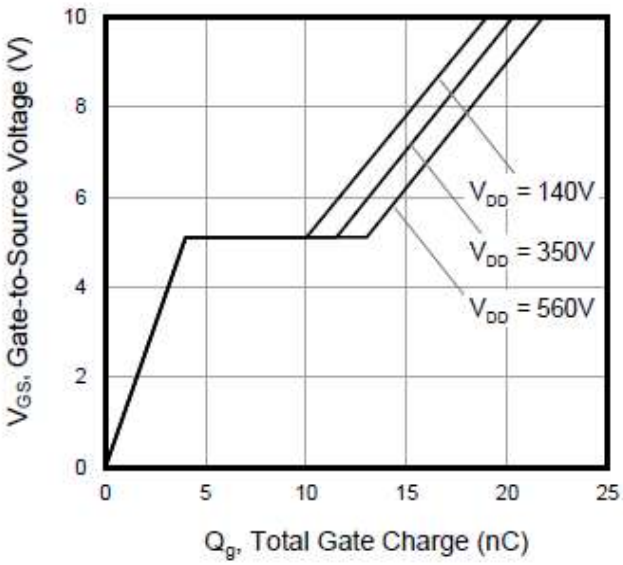
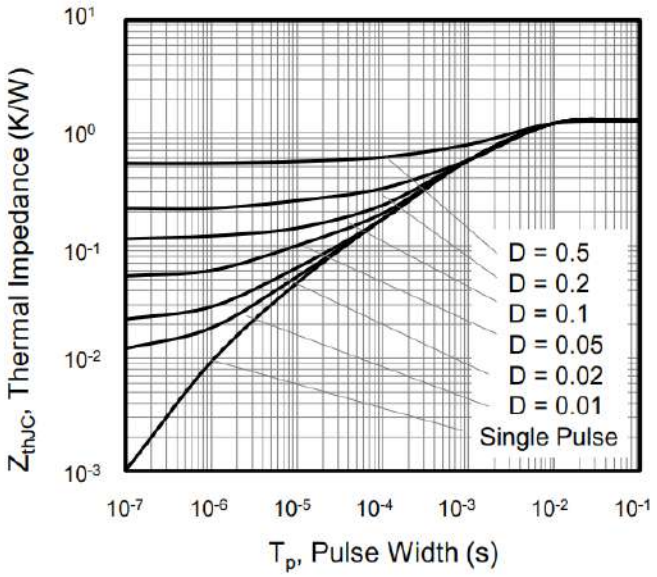


Figure9. Transient Thermal Impedance
TO-252



Test Circuits and Waveforms

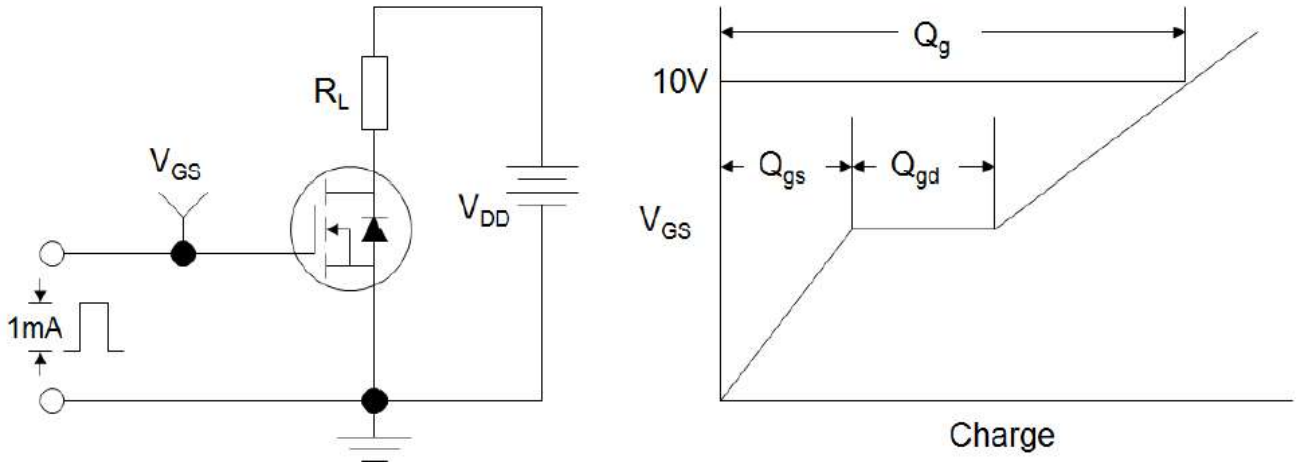


Figure10.
Gate Charge Test Circuit and Waveform

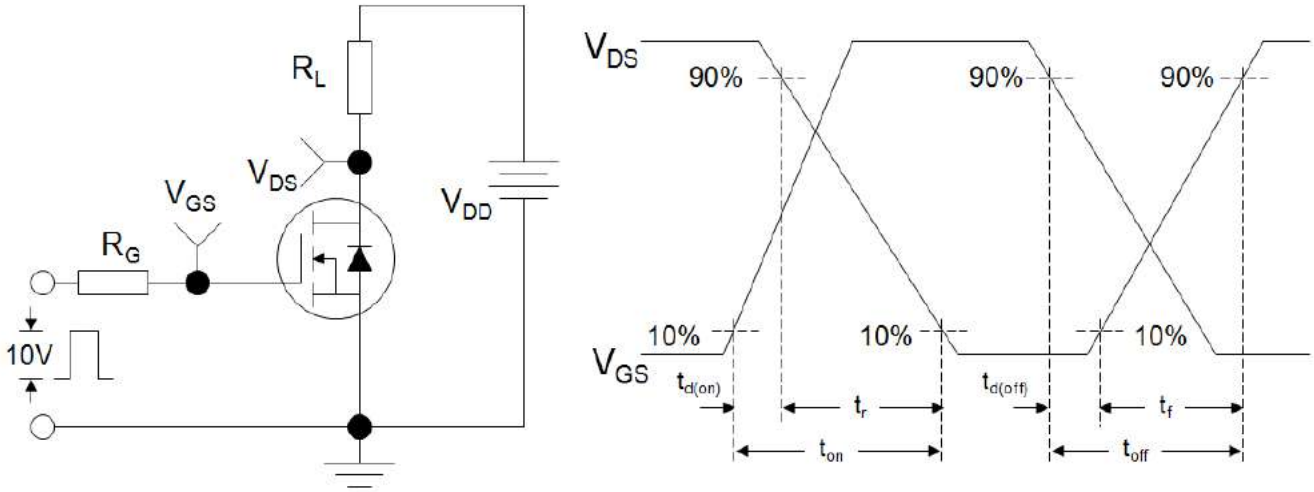


Figure11.
Resistive Switching Test Circuit and Waveform

Test Circuits and Waveforms

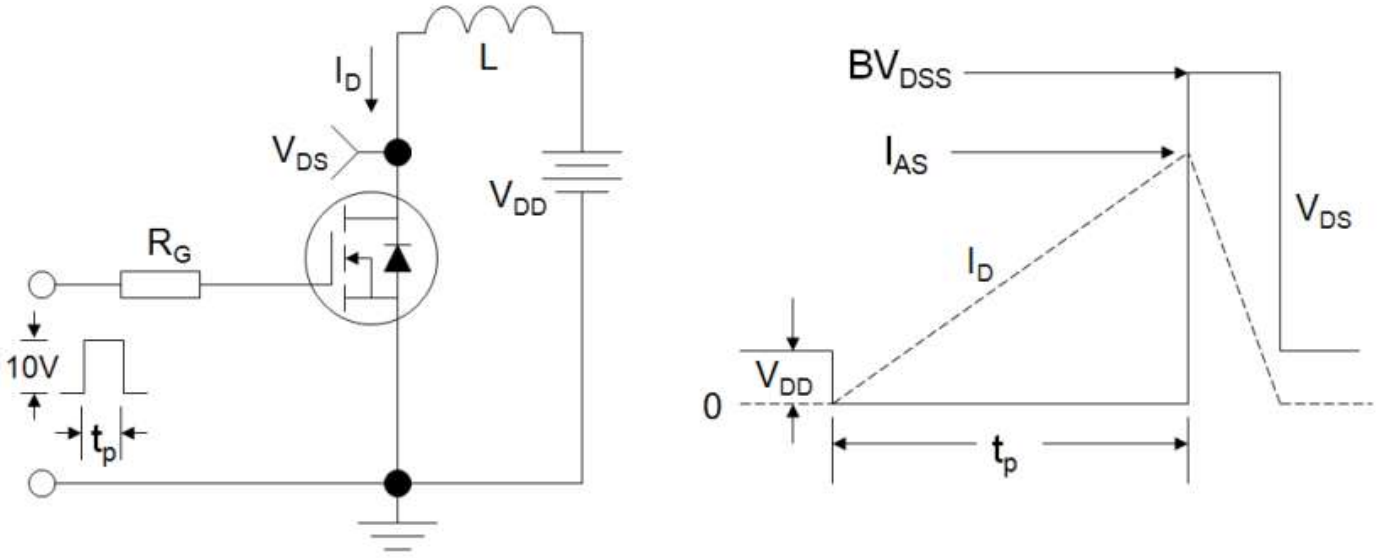
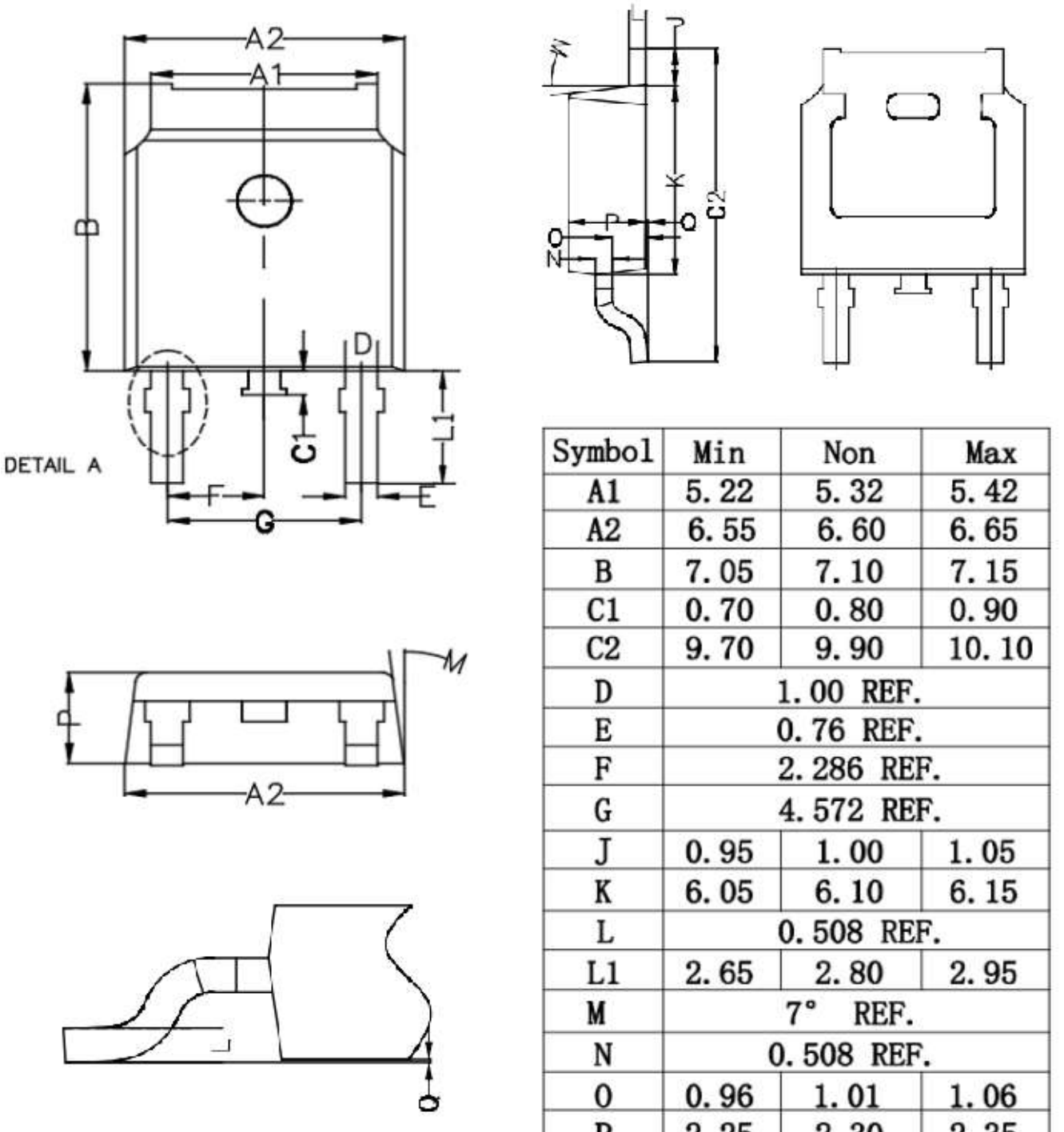


Figure12.Unclamped Inductive Switching Test Circuit and Waveform

Package outline drawing

Unit:mm



Symbol	Min	Non	Max
A1	5.22	5.32	5.42
A2	6.55	6.60	6.65
B	7.05	7.10	7.15
C1	0.70	0.80	0.90
C2	9.70	9.90	10.10
D		1.00 REF.	
E		0.76 REF.	
F		2.286 REF.	
G		4.572 REF.	
J	0.95	1.00	1.05
K	6.05	6.10	6.15
L		0.508 REF.	
L1	2.65	2.80	2.95
M		7° REF.	
N		0.508 REF.	
O	0.96	1.01	1.06
P	2.25	2.30	2.35
Q	0.00	0.05	0.10

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