REASUNOS

RSM120025W

N-Channel Enhancement Mode

V_{DS}	=	1200 V
$R_{DS(on)}$	=	25 mΩ
I_{DS}@25℃	=	90A

Features

- High Blocking Voltage with low On-Resistance
- High Speed Switching with Low Capacitances
- Easy to Parallel and Simple to Drive
- Avalance Ruggedness

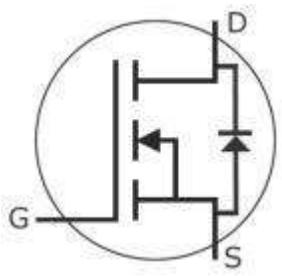
Benefits

- Higher System Efficiency
- Reduced Cooling Requirements
- Increased Power Density
- Increased System Switching Frequency

Applications

- Solar Inverters
- Switch Mode Power Supplies
- High Voltage DC/DC Converters
- Motor Drivers
- Pulsed Power Applications

Chip Outline



Part Number	Package
RSM120025W	TO-247-3

Maximum Ratings (T_C=25˚C unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{DSmax}	Drain-Source Voltage	1200	V	V_{GS}=0V, I_{DS}=100μA	
V_{GSmax}	Gate-Source Voltage	-10/+25	V	Absolute maximum values	
V_{GSop}	Gate-Source Voltage	-5/+20	V	Recommended operational values	
I_D	Continuous Drain Current	90	A	V_{GS}=20V, Tc=25℃	
		60	A	V_{GS}=20V, Tc=100℃	
$I_{D(pulse)}$	Pulsed Drain Current	250	A	Pule width t_p limited by T_{jmax}	
P_D	Power Dissipation	463	W	Tc=25℃ , T_J=150℃	
T_J,T_{STG}	Operating Junction and Storage Temperature	-40 to +150	℃		
T_L	Solder Temperature	260	℃	1.6mm(0.063”) from case for 10s	

Electrical Characteristics(T_C=25°C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1200	/	/	V	V_{GS}=0V, I_{DS}=100μA	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	2.4	4	V	V_{DS}=V_{GS}, I_{DS}=15mA	
			1.8	/		V_{DS}=V_{GS},I_{DS}=15mA, T_J=150℃	
I_{DSS}	Zero Gate Voltage Drain Current	/	1	100	μA	V_{DS}=1200V, V_{GS}=0V	
I_{GSS}	Gate-Source Leakage Current	/		250	nA	V_{DS}=0V, V_{GS}=20V	
$R_{DS(on)}$	Drain-Source On-State Resistance	/	25	34	mΩ	V_{GS}=20V, I_D=50A	
		/	43			V_{GS}=20V, I_D=50A, T_J=150℃	
g_{fs}	Transconductance	/	22.8	/	S	V_{DS} = 20 V, I_D = 50 A	
		/	21.2	/		V_{DS}=20V, I_D = 50A, T_J= 150℃	
C_{iss}	Input Capacitance	/	3600	/	pF	V_{GS}=0V	
C_{oss}	Output Capacitance	/	240	/		V_{DS}=1000V	
C_{rss}	Reverse Transfer Capacitance	/	16	/		f=1MHz	
E_{oss}	C_{oss} Stored Energy	/	122	/	μJ	V_{AC}=25mV	
t_{don}	Turn-On Delay Time	/	16	/	ns	V_{DS}=800V,V_{GS}=-5V/20V	
t_r	Rise Time	/	16.2	/		I_D=30A,R_g=2.5Ω	
t_{doff}	Turn-Off Delay Time	/	33	/		R_L=2.5Ω	
t_f	Fall Time	/	7.8	/		(TO-247-3Package)	
E_{ON}	Turn-On Switching Energy	/	1.8	/	μJ	V_{DS}=800V,V_{GS}=-5V/20V	
E_{OFF}	Turn-Off Switching Energy	/	1.5	/		I_D=30A,R_g=2.5Ω,L=200μH (TO-247-3Package)	
R_G	Internal Gate Resistance	/	2.0	/	Ω	f=1MHz open drain	
Q_{gs}	Gate Charge Total	/	54	/	nC	V_{DS}=800V	
Q_{gd}	Gate to Source Charge	/	29	/		V_{GS}=-5V/20V	
Q_g	Gate to Drain Charge	/	195	/		I_D=30A	

Reverse Diode Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	3.6		V	V_{GS}=-5V, I_F=25A	
		3.3			V_{GS}=-5V, I_F=25A， T_J=150℃	
I_S	Continuous Diode Forward Current		90	A	T_C=25℃	
t_{rr}	Reverse Recover time	55		ns	V_{GS}=-5V,I_{SD}=25A,V_R=800V	
Q_{rr}	Reverse Recovery Charge	320		nC		
I_{rrm}	Peak Reverse Recovery Current	10.7		A		

Reverse Diode Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance	0.24	0.28	℃/W		

Typical Performance

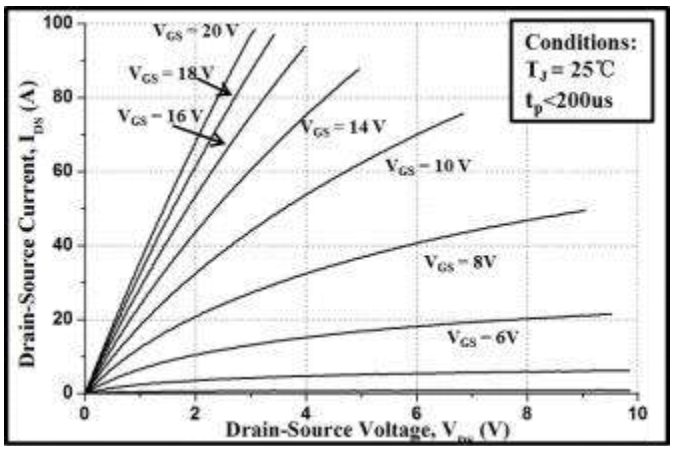


Figure 1. Typical Output Characteristics T_J=25℃

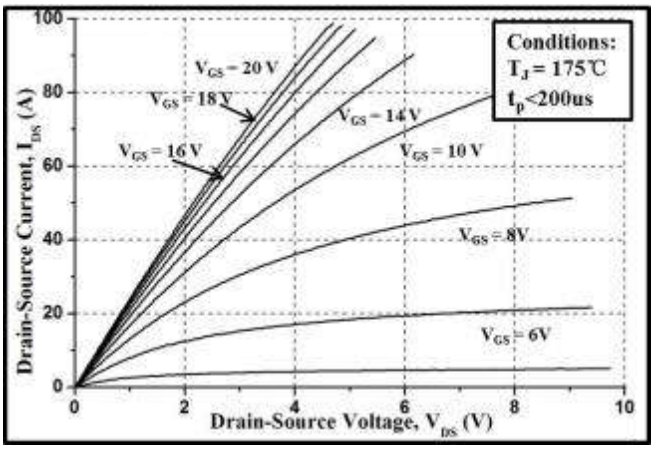


Figure 2. Typical Output Characteristics T_J=175℃

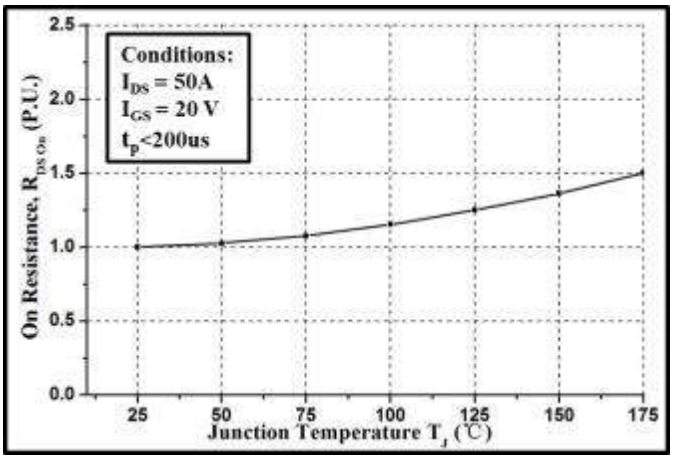


Figure 3. Normalized On-Resistance vs. Temperature

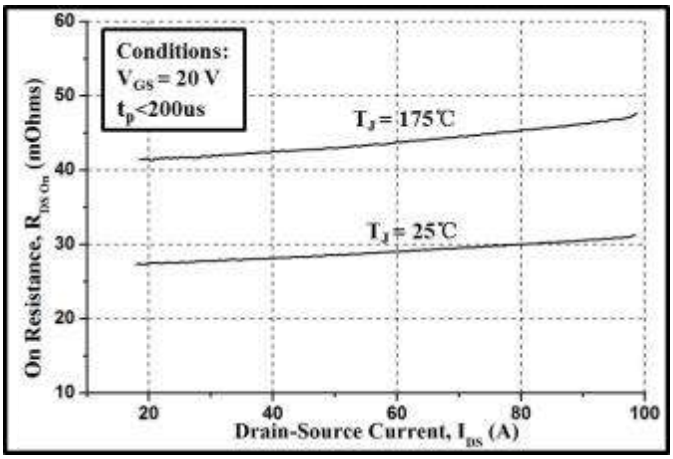


Figure 4. On-Resistance vs. Drain Current

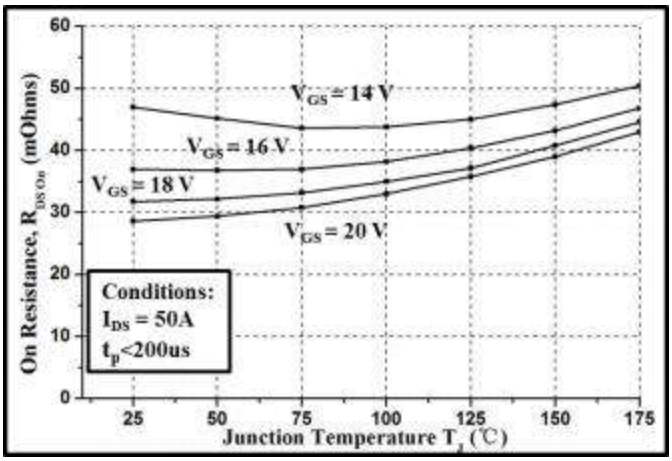


Figure 5. On-Resistance vs. Temperature

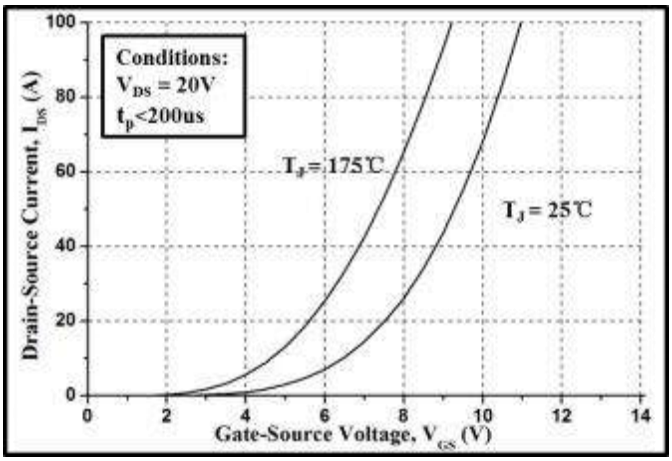


Figure 6. Typical Transfer Characteristics

Typical Performance

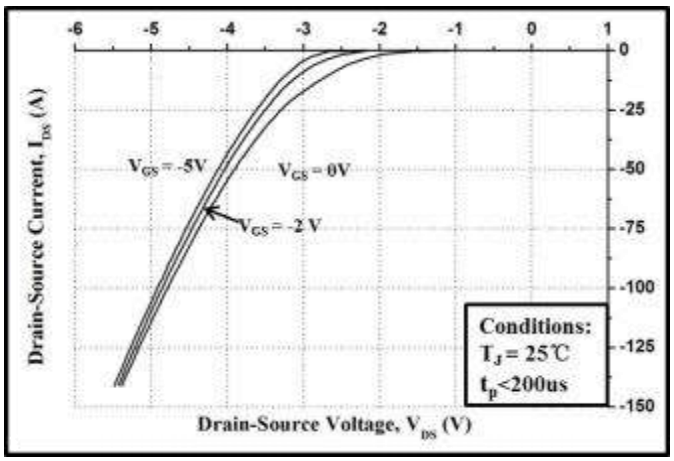


Figure 7. Body Diode Characteristics at 25℃

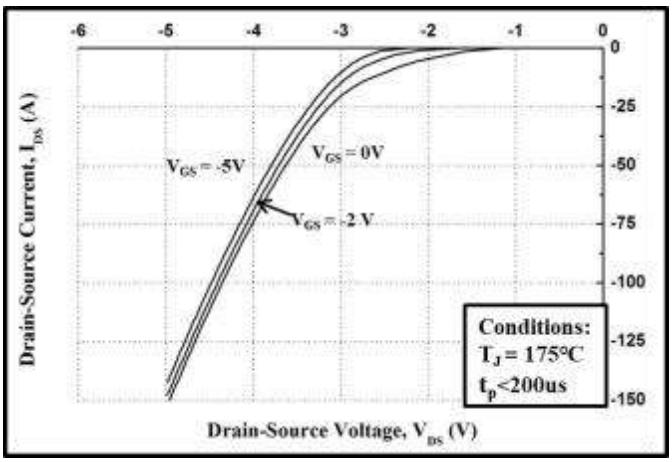


Figure 8. Body Diode Characteristics at 175℃

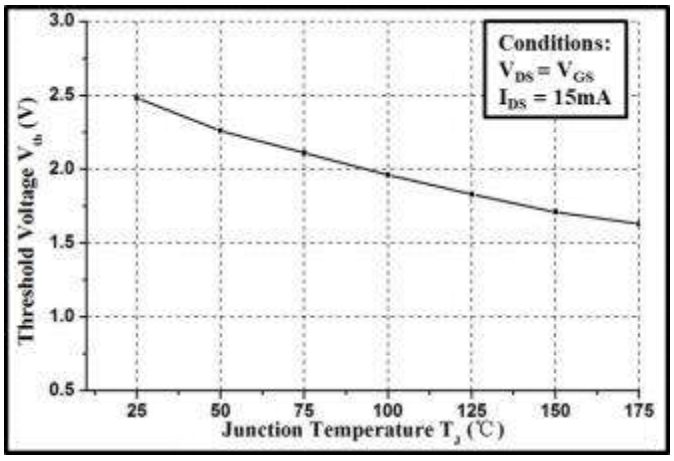


Figure 9. Gate Threshold Voltage vs. Temperature

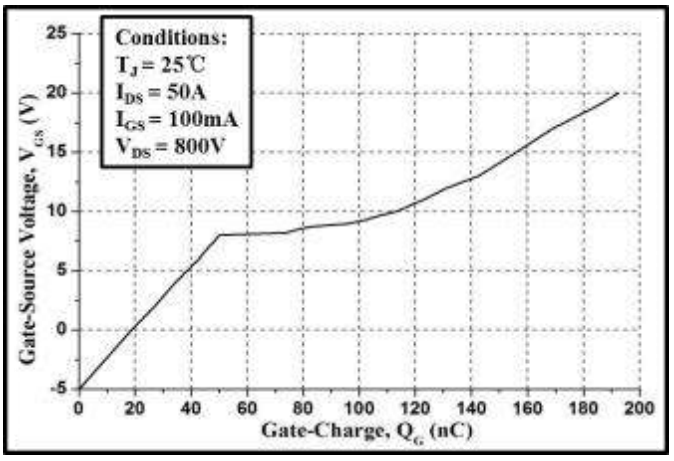


Figure 10. Gate Charge Characteristic

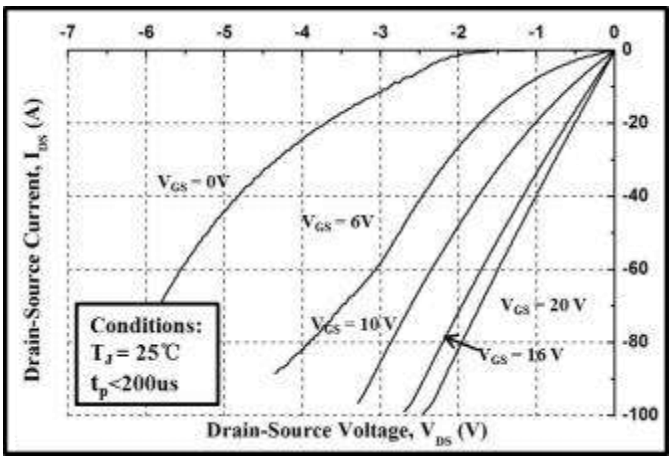


Figure 11. 3rd Quadrant Characteristics at 25° C

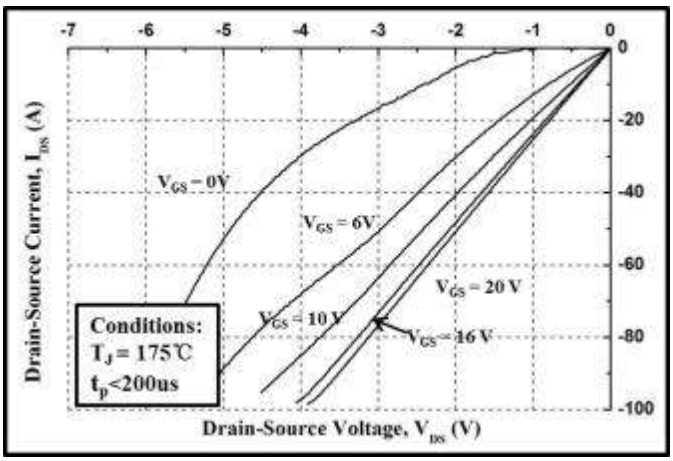


Figure 12. 3rd Quadrant Characteristics at 175° C

Typical Performance

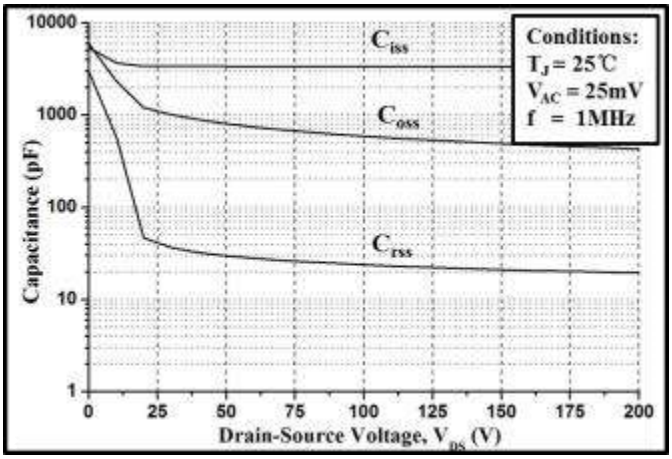


Figure 13. Capactances vs. Drain-Source Voltage

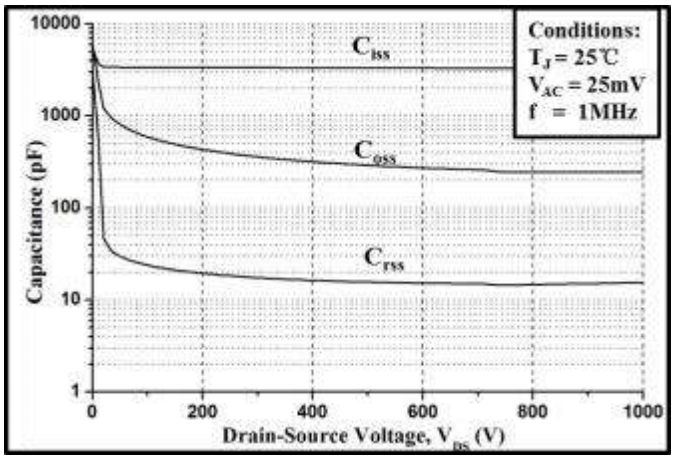


Figure 14. Capactances vs. Drain-Source Voltage

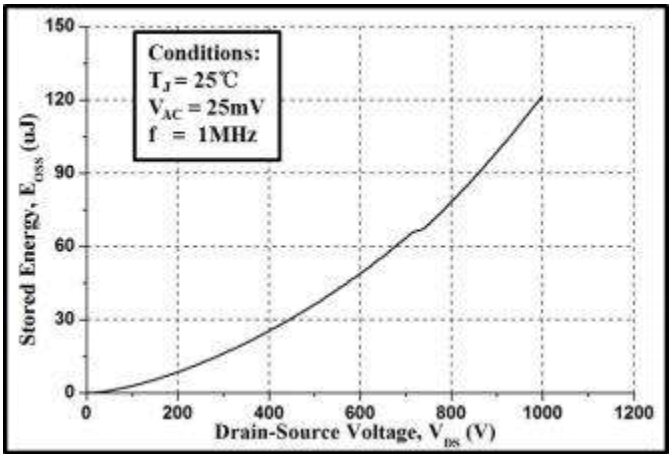
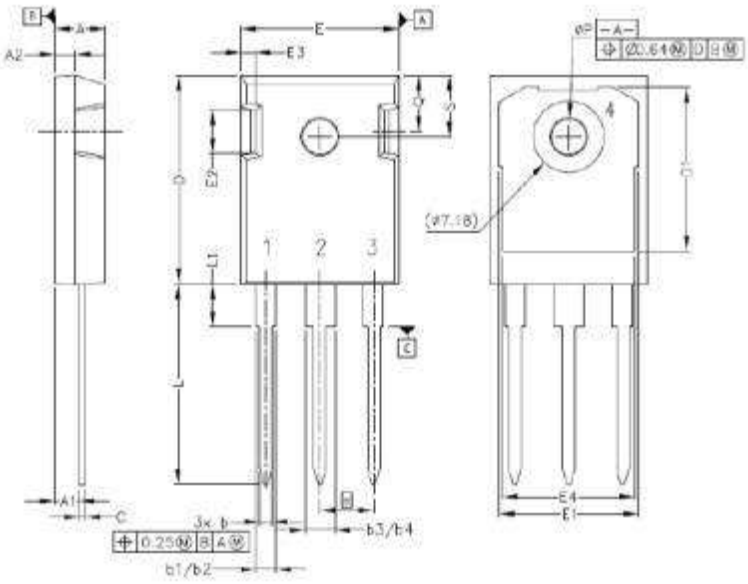
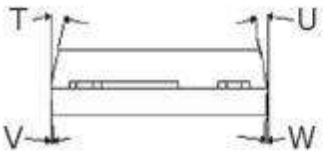


Figure 15. Output Capacitor Stored Energy

Package Dimension



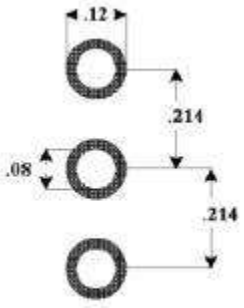


Pinout Information:

- Pin 1 = Gate
- Pin 2, 4 = Drain
- Pin 3 = Source

POS	Inches		Millimeters	
	Min	Max	Min	Max
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.042	.052	1.07	1.33
b1	.075	.095	1.91	2.41
b2	.075	.085	1.91	2.16
b3	.113	.133	2.87	3.38
b4	.113	.123	2.87	3.13
c	.022	.027	0.55	0.68
D	.819	.831	20.80	21.10
D1	.640	.695	16.25	17.65
D2	.037	.049	0.95	1.25
E	.620	.635	15.75	16.13
E1	.516	.557	13.10	14.15
E2	.145	.201	3.68	5.10
E3	.039	.075	1.00	1.90
E4	.487	.529	12.38	13.43
e	.214 BSC		5.44 BSC	
N	3		3	
L	.780	.800	19.81	20.32
L1	.161	.173	4.10	4.40
ØP	.138	.144	3.51	3.65
Q	.216	.236	5.49	6.00
S	.238	.248	6.04	6.30
T	9°	11°	9°	11°
U	9°	11°	9°	11°
V	2°	8°	2°	8°
W	2°	8°	2°	8°

Recommended Solder Pad Layout



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