REASUNOS

RSM120040W

N-Channel SiC Power MOSFET

V_{DS}	=	1200	V
$R_{DS(on)}$	=	40	mΩ
I_D@25℃	=	68	A

Features

- High Blocking Voltage with Low On-Resistance
- High Speed Switching with Low Capacitance
- Easy to Parallel and Simple to Drive

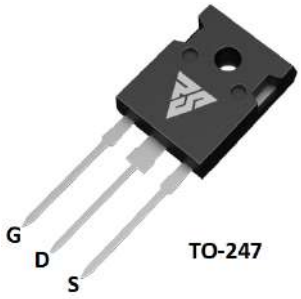
Benefits

- Higher System Efficiency
- Reduced Cooling Requirements
- Increased Power Density
- Increased System Switching Frequency

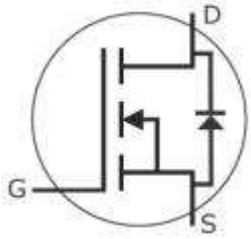
Applications

- Renewable Energy
- EV Battery Chargers
- High Voltage DC/DC Converters
- Switch Mode Power Supplies

Package



TO-247



Part Number	Package
RSM120040W	TO-247-3

Maximum Ratings (T_C=25℃ unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{DSmax}	Drain-Source Voltage	1200	V	V_{GS}=0V, I_D=100μA	
V_{GSmax}	Gate-Source Voltage	-8/+22	V	Absolute maximum values	
V_{GSop}	Gate-Source Voltage	-4/+18	V	Recommended operational values	
I_D	Continuous Drain Current	68	A	V_{GS}=18V, T_c=25℃	
		49		V_{GS}=18V, T_c=100℃	
$I_{D(pulse)}$	Pulsed Drain Current	100	A	Pulse width t_p limited by T_{Jmax}	
P_D	Power Dissipation	340	W	T_c=25℃, T_J=175℃	
T_J, T_{STG}	Operating Junction and Storage Temperature	-55 to +175	℃		

Electrical Characteristics (T_C=25℃ unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1200	/	/	V	V_{GS}=0V, I_D=100μA	
$V_{GS(th)}$	Gate Threshold Voltage	1.9	2.6	4.0	V	V_{DS}=V_{GS}, I_D=9.5mA	
		/	1.8	/		V_{DS}=V_{GS}, I_D=9.5mA, T_J=175℃	
I_{DSS}	Zero Gate Voltage Drain Current	/	1	100	μA	V_{DS}=1200V, V_{GS}=0V	
I_{GSS+}	Gate-Source Leakage Current	/	10	250	nA	V_{DS}=0V, V_{GS}=22V	
I_{GSS-}	Gate-Source Leakage Current	/	10	250	nA	V_{DS}=0V, V_{GS}=-8V	
$R_{DS(on)}$	Drain-Source On-State Resistance	/	40	53	mΩ	V_{GS}=18V, I_D=33.3A	
		/	65	/		V_{GS}=18V, I_D=33.3A, T_J=175℃	
g_{fs}	Transconductance	/	21	/	S	V_{DS}=20V, I_D=33.3A	
		/	17.5	/		V_{DS}=20V, I_D=33.3A, T_J=175℃	
C_{iss}	Input Capacitance	/	2070	/	pF	V_{GS}=0V	
C_{oss}	Output Capacitance	/	112	/		V_{DS}=1000V	
C_{rss}	Reverse Transfer Capacitance	/	11	/		f=1MHz	
E_{oss}	C_{oss} Stored Energy	/	66	/	μJ	V_{AC}=25mV	
E_{ON}	Turn-On Switching Energy	/	1410	/	μJ	V_{DS}=800V, V_{GS}=-4V/18V	
E_{OFF}	Turn-Off Switching Energy	/	750	/		I_D=33A, $R_{G(ext)}$=2.5Ω, L=100μH	
$t_{d(on)}$	Turn-On Delay Time	/	17	/	ns	V_{DS}=800V, V_{GS}=-4V/18V, I_D=33A $R_{G(ext)}$=2.5Ω, R_L=20Ω	
t_r	Rise Time	/	58	/			
$t_{d(off)}$	Turn-Off Delay Time	/	26	/			
t_f	Fall Time	/	15	/			
$R_{G(int)}$	Internal Gate Resistance	/	4.9	/	Ω	f=1MHz, V_{AC}=25mV	
Q_{GS}	Gate to Source Charge	/	34	/	nC	V_{DS}=800V V_{GS}=-4V/18V I_D=33A	
Q_{GD}	Gate to Drain Charge	/	20	/			
Q_G	Total Gate Charge	/	121	/			

Reverse Diode Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	4.5	/	V	V_{GS}=-4V, I_{SD}=10A	
		4.2	/		V_{GS}=-4V, I_{SD}=10A, T_J=175℃	
I_S	Continuous Diode Forward Current	/	51	A	T_C= 25℃	
t_{rr}	Reverse Recover Time	38	/	ns	V_R=800V, I_{SD}=20A	
Q_{rr}	Reverse Recovery Charge	109	/	nC		
I_{rrm}	Peak Reverse Recovery Current	5	/	A		

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.44	/	℃/ W		
$R_{\theta JA}$	Thermal Resistance from Junction to Ambient	/	40			

Typical Performance

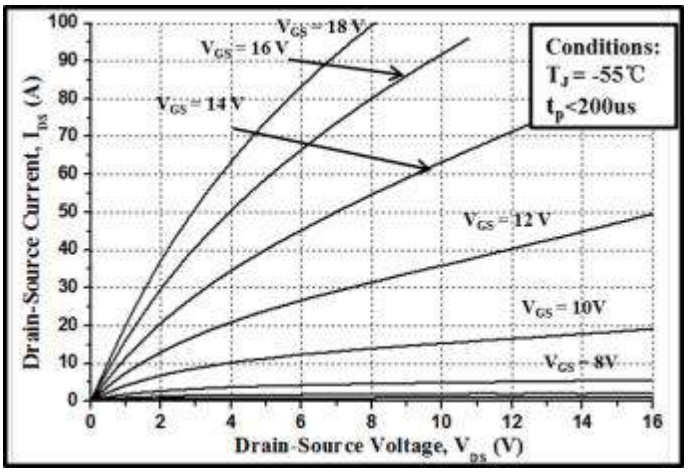


Figure 1. Output Characteristics T_J = -55℃

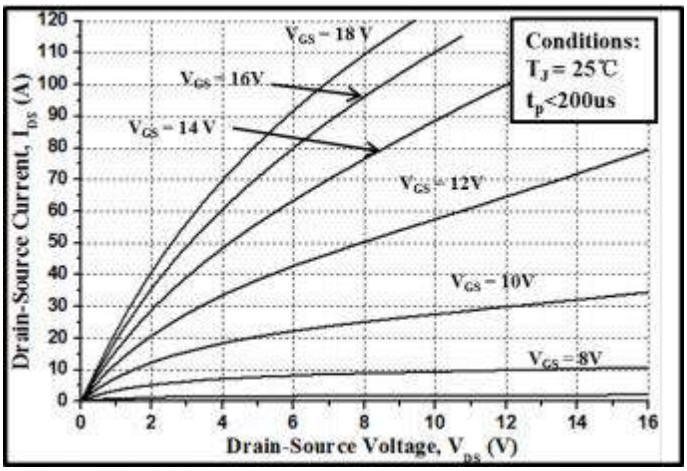


Figure 2. Output Characteristics T_J = 25℃

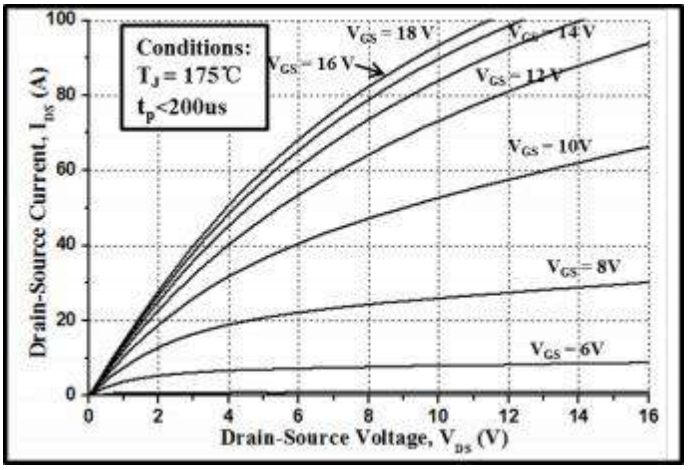


Figure 3. Output Characteristics T_J = 175℃

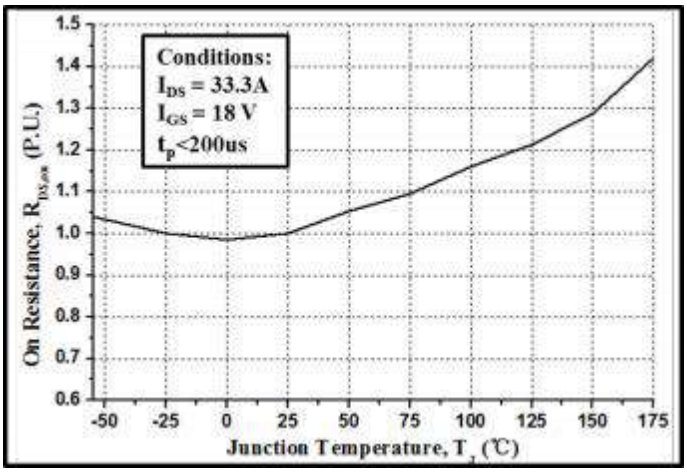


Figure 4. Normalized On-Resistance vs. Temperature

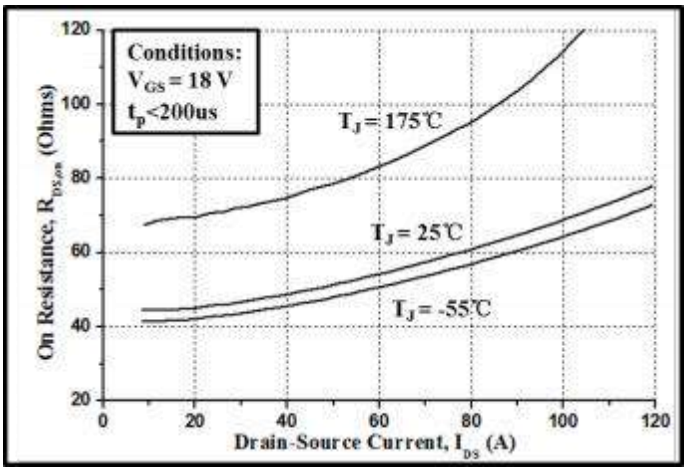


Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

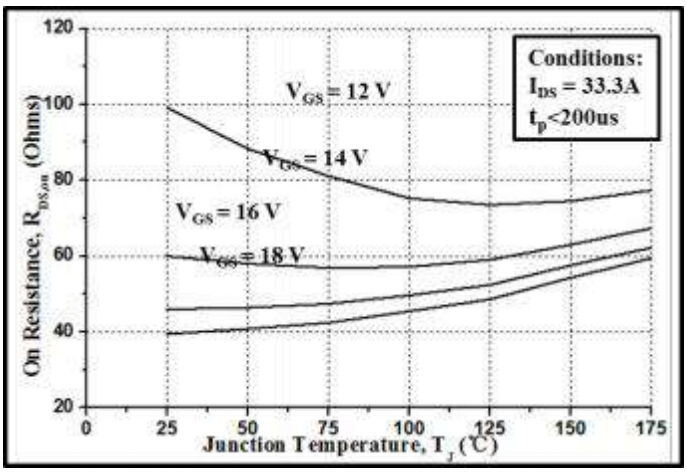


Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

Typical Performance

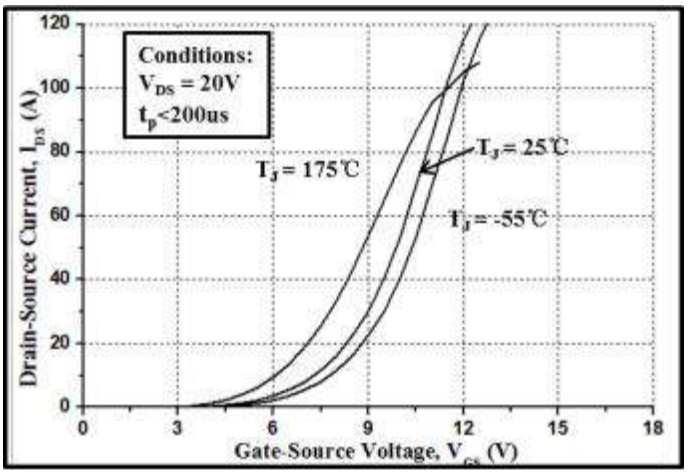


Figure 7. Transfer Characteristic for Various Junction Temperatures

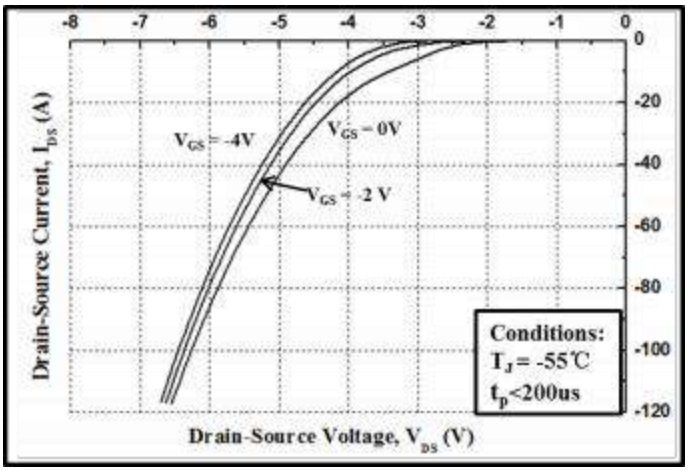


Figure 8. Body Diode Characteristic at -55℃

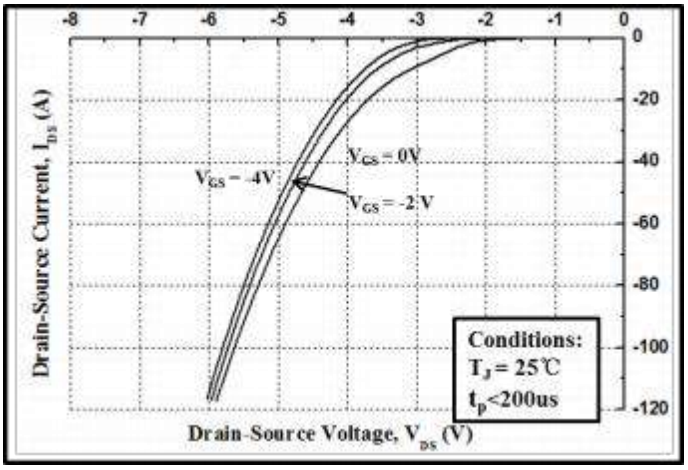


Figure 9. Body Diode Characteristic at 25℃

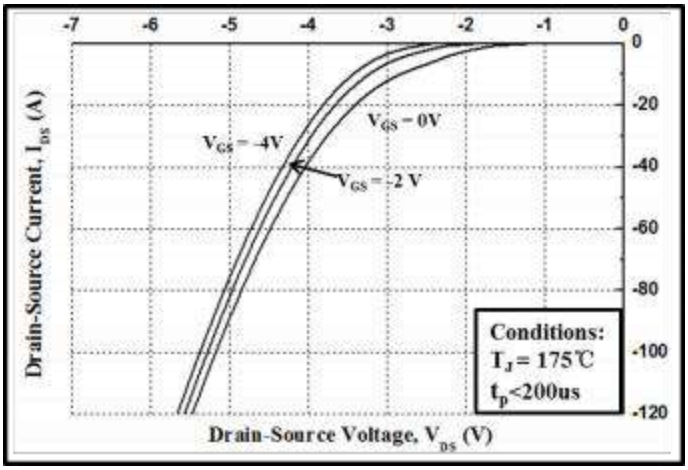


Figure 10. Body Diode Characteristic at 175℃

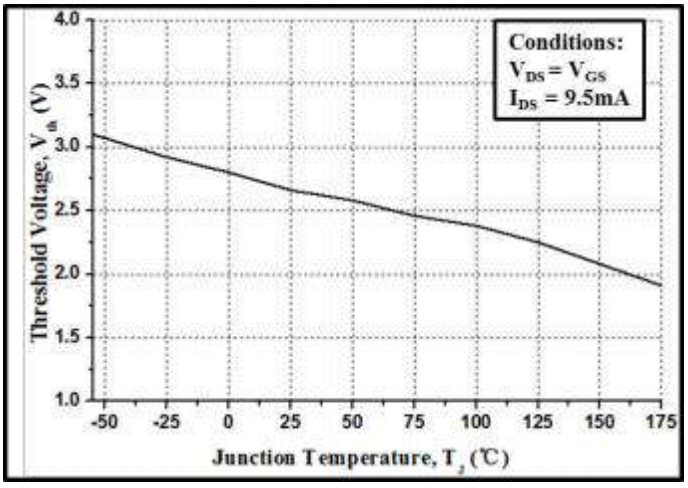


Figure 11. Threshold Voltage vs. Temperature

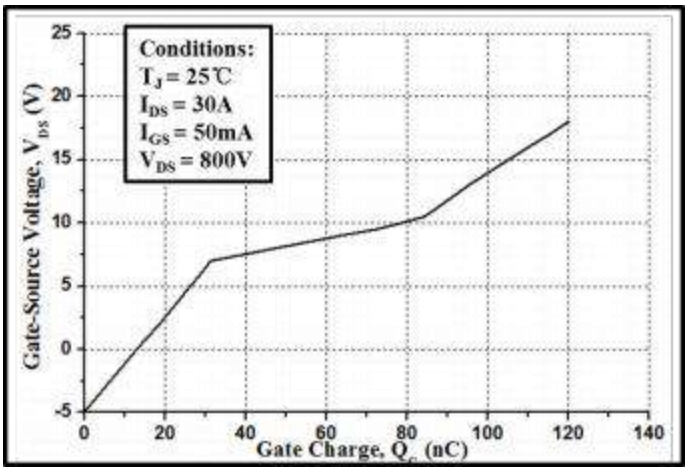


Figure 12. Gate Charge Characteristics

Typical Performance

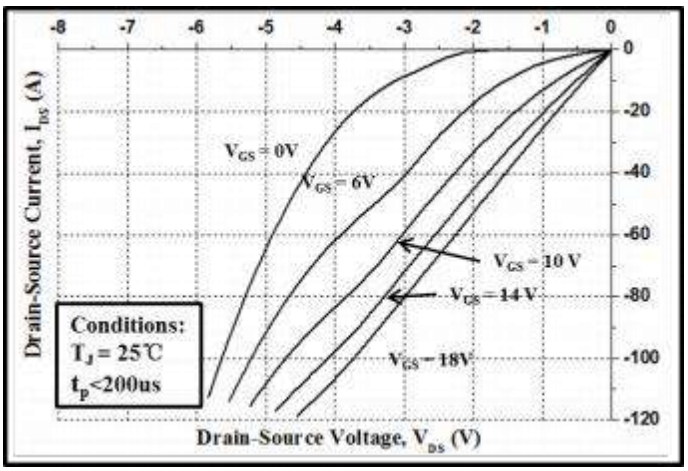


Figure 13. 3rd Quadrant Characteristic at 25℃

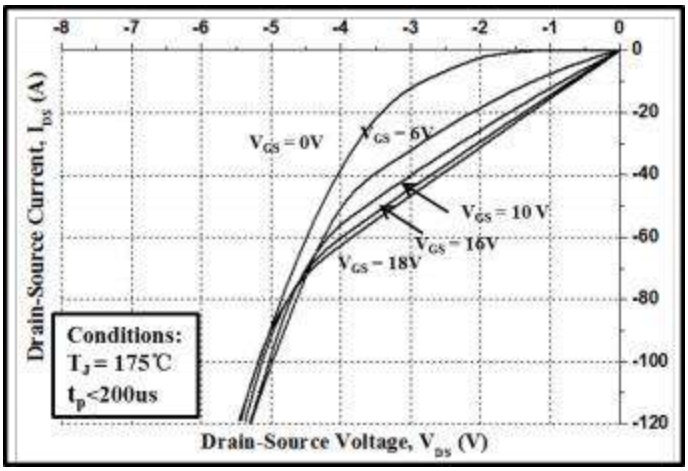


Figure 14. 3rd Quadrant Characteristic at 175℃

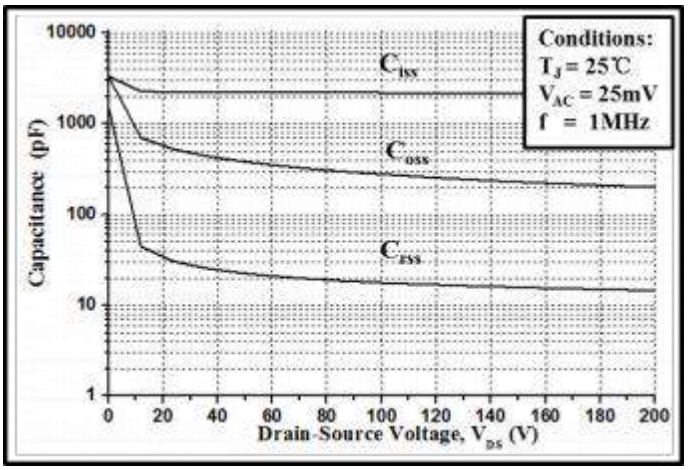


Figure 15. Capacitances vs. Drain-Source Voltage (0 - 200V)

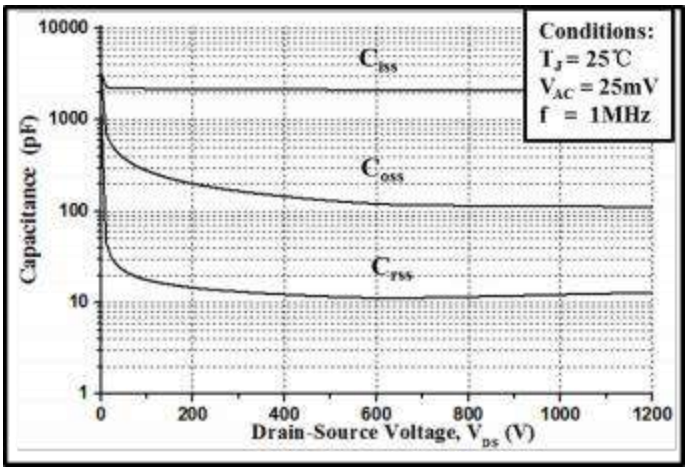
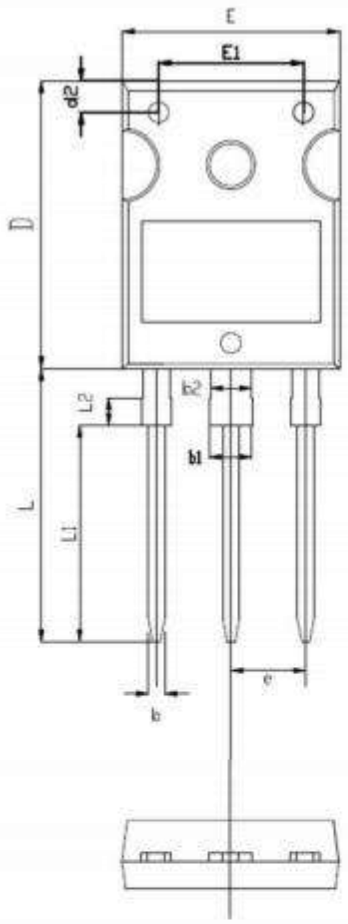
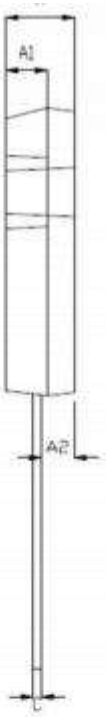
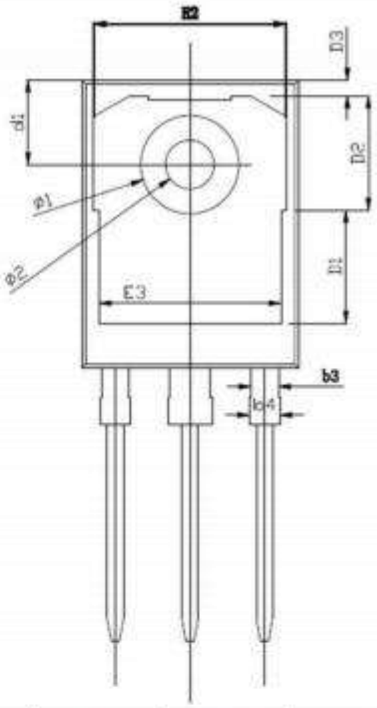


Figure 16. Capacitances vs. Drain-Source Voltage (0 - 1200V)

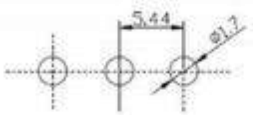
Package Dimensions







RECOMMENDED LAND PATTERN



UNIT: mm

	MIN	NOM	MAX
A	4.80	5.00	5.20
A1	2.80	3.00	3.20
A2	2.26	2.41	2.56
b	1.10	1.20	1.30
b1	2.90	-	3.20
b2	2.90	3.00	3.10
b3	1.90	2.00	2.10
b4	2.00	-	2.20
c	0.50	0.60	0.70
D	20.80	21.00	21.20
D1		8.23	
D2		8.32	
D3		1.17	
d1	6.00	6.15	6.30
d2	2.20	2.30	2.40
E	15.60	15.80	16.00
E1		10.50	
E2		14.02	
E3		13.50	
e	5.34	5.44	5.54
L	19.72	19.92	20.12
L1		15.79	
L2		1.98	
ø1	7.10	7.19	7.30
ø2	3.50	3.60	3.70

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